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INVESTIGATION OF REFRACTORY DIELECTRICS FOR INTEGRATED CIRCUITS

by V. Y. Doo and D. R. Kerr

Prepared by
INTERNATIONAL BUSINESS MACHINES CORPORATION
Cambridge, Mass.
for Electronics Research Center

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PURPOSE

The purpose of this contract is to accomplish the work set forth below:

1. Survey and analyze the literature to determine the most promising material superior to silicon dioxide, that will serve as a dielectric and passivating film for integrated circuits.

2. Develop an insulator with a high softening point not reactive with semiconductor material at temperatures up to 1300°C. The insulator shall:
   a. form as good a dielectric as silicon dioxide in making metal — dielectric-semiconductor capacitors.
   b. mask against diffusion of n-type and p-type impurities, and
   c. provide a passivating surface for integrated circuits.

3. Design and build an integrated circuit based upon the results of work under item 2.

ABSTRACT

Extensive literature survey and analysis on silicon nitride made prior to this contract indicate that many of its properties are superior to silicon dioxide and that it meets the requirements of this contract.

Growth parameters for pyrolytic silicon nitride such as nucleation, reactant composition, substrate temperature, substrate preparation and carrier gas were studied.

Measurements were made in MNS (metal-nitride-silicon) and MNOS (metal-nitride-oxide-silicon) samples for surface charge density, electronic leakage and dielectric constant determination. The index of refraction and 48% HF etch rate were also measured.

The masking property of silicon nitride for dopants which silicon dioxide fails to mask were investigated. Photolithographic techniques were developed so that conventional photoresist could be used.

Silicon nitride together with silicon dioxide was used to passivate silicon integrated circuit transistors and diodes. The integrated circuits were thermally and electrically stressed, and the results on H_{FE} and junction breakdowns changes were recorded.

LITERATURE SURVEY AND ANALYSIS

Extensive literature survey and analysis on silicon nitride had been made at IBM Component Laboratory prior to this contract. This information has been voluntarily submitted to NASA for review as included in the technical proposal R.E.P.N. R & D 66-120, "Investigation of Refractory Dielectrics for Integrated Circuits," January 5, 1966.

The results from the IBM investigation prior to April 1, 1966 on silicon nitride strongly indicate that many of its physical properties are superior to silicon dioxide and that it meets the requirements of this contract. Therefore, it was decided that the insulating material to be developed would be limited to silicon nitride. This decision was agreeable to NASA representative Dr. P. Klein and Mr. R. Trent during their visit to the IBM Components Division, Development Laboratory, East Fishkill, N. Y. on April 13, 1966. During this meeting, the program for development of silicon nitride was discussed and was mutually agreed upon by the NASA and IBM representatives. This program includes the investigation of growth, quality, diffusion masking, and integrated circuit application. Growth study would cover nucleation study, growth kinetic study, and alternate silicon nitride and silicon dioxide layer growth. Quality evaluation includes electrical measurements, chemical composition analysis and chemical etch study. The diffusion masking study includes the photo-etch development as well as the investigation of the masking against dopant diffusion. The integrated circuit applications of silicon nitride film have been pursued after the above items were investigated.

A comparison of physical properties of SiO_2, Si_3N_4, and $Si\text{-}O_x\text{-}N_y$ is given in the following summary. Some numbers in this summary are taken from the literature, while others are a result of this investigation. Following the summary, typical deposition conditions for the films to be discussed in this report are given.

Summary of the Physical Properties of SiO_2, Si_3N_4 and $Si\text{-}O_x\text{-}N_y$

Structure	SiO_2 amorphous	Si_3N_4 crystalline	Si_3N_4 amorphous	$Si\text{-}O_x\text{-}N_y$ amorphous
Melting Point (^oC)	~1600	~1900	-	-
Density (g cm^{-3})	2.2	3.4	3.1	-
Index of Refraction	1.46	2.1	2.05	1.60-1.88
Dielectric Constant	3.8-3.9	9.4	7.5	4.77-6.12
Dielectric Strength (V cm^{-1})	$\sim 5 \times 10^6$	-	$\sim 1 \times 10^7$	$\sim 5 \times 10^6$
Infrared absorption band, (μ)	9.3	10.6	11.5-12.0	9.3 and 12.0
Energy gap (e.v.)	8	3.9-4.0	~5.0	-
Thermal Expansion Coeff. ($^oC^{-1}$)	5.6×10^{-7}	$3.0 - 3.5 \times 10^{-6}$	-	-
Thermal Conductivity (cal cm^{-1} sec^{-1} $^oC^{-1}$	0.0032	0.067	-	-
D.C. Resistivity (ohm-cm)				
@ 25°C	10^{14}-10^{16}	10^{15}	$\sim 10^{14}$	
@ 250°C	-	-		
@ 300°C	-	-		
@ 500°C		$\sim 10^{13}$	$\sim 2 \times 10^{13}$	
Etch Rate in 10:1 NH_4F:HF (Å/min)	1000	$\ll 0.1$	5-10	33-400

Growth of impervious Si_3N_4 films for integrated circuit and device passivation

Reactor Cross-section (mm^2)	80 x 50
Susceptor cross-section (mm^2)	76 x 16
Inlet gases = SiH_4 (ml/min)	1
NH_3 (ml/min)	20
Carrier gas, N_2 (ℓ/min)	40
Substrate temperature (^oC):	
Deposit on completed integrated circuit wafers	800^oC
Deposit on wafers prior to device fabrication	900^oC
Growth rate (Å/min)	150-220
Etch rate of Si_3N_4 in 48% HF (Å/min)	100-120

When deposition is made on wafers prior to device fabrication, a thin layer of thermal SiO_2 (≈300 Å) is usually grown on silicon substrates prior to the Si_3N_4 deposition. The in-situ thermal SiO_2 is preferred although externally grown SiO_2 can be used. In-situ oxidation conditions are:

Dry O_2 fills the entire system prior to heating.

Dry O_2 flowrate 500 cc/min

Substrate temperature 25^o - 1000^oC 3 min

1000^oC 17 min

1000^o-850^oC 5 min

Flush with N_2 40 ℓ/min for 15 min at 850^oC. Then the deposition of Si_3N_4 proceeds under the condition described above.

Pyrolytic SiO_2 is usually used as the mask for photoetching Si_3N_4. Conditions for depositing SiO_2 vary widely. Two typical SiO_2 deposition systems are:

A. $SiCl_4$ - O_2 - H_2 system

$SiCl_4$ flowrate	50 cc/min
O_2 flowrate	300 cc/min
H_2 flowrate	30 ℓ/min
Substrate temperature	800^oC
Growth rate	900 Å/min
Etch rate in 10:1 buffered HF	50 Å/sec

B. $SiH_4 - O_2 - H_2$ system

SiH_4 flowrate	3 cc/min
O_2 flowrate	30 cc/min
H_2 flowrate	30 ℓ/min
Substrate temperature	450°C
Growth rate	340 Å/min
Etch rate in 10:1 buffered HF	200 Å/sec

1.0 SILICON NITRIDE GROWTH PROCESS

The pyrolytic deposition of silicon nitride by the reaction of silane and ammonia in a stream of hydrogen gas has been reported earlier.[1] The complete chemical reaction can be represented by

$$3\ SiH_4 + 4\ NH_3 \quad Si_3N_4 + 12\ H_2.$$

Silane starts to decompose at about 500°C. To suppress the premature decomposition of silane, hydrogen was injected into the reactor as carrier gas. When the reaction occurred in other carrier gases such as helium, nitrogen and argon, a layer of silicon powder was formed on the reactor wall, thus obscuring the view of the sample. However, it was later found that this difficulty was overcome by using a larger flow of carrier gas which reduces the atmospheric temperature in the reactor, thus prohibiting or greatly minimizing the premature decomposition of silane. Because the molecular weight of nitrogen (or argon) is comparable to, while that of hydrogen (or helium) is much less than either silane or ammonia, the gas mixture in the reactor with SiH_4 - NH_3 - N_2 system would be more homogeneous than the SiH_4 - NH_3 - H_2 system, thus better uniform film growth. Besides, the SiH_4 - NH_3 - N_2 is much less hazardous to operate than the SiH_4 - NH_3 - H_2 system. The electrical properties of the silicon nitride films, which is the major determining factor, grown in nitrogen are comparable to if not better than that in hydrogen. The later part of this investigation is therefore devoted mainly to nitrogen.

1.1 APPARATUS AND MEASUREMENT METHODS

The apparatus used in this work was designed previously.[1] A series of modifications were made to meet the requirement for improved growth control. The feed system consists of a series of valves and flowmeters for controlling input gases, i.e., silane, ammonia and carrier gas. Since the input gases are corrosive in nature, the entire feed system was made of stainless steel except the flowmeters. The feed system was made gas-tight and could be evacuated up to the input gas cylinder valves. Figure 1 shows the flow chart of the feed system including the latest modifications. In addition to the provisions for silane, ammonia and carrier gas, the valves and flowmeters for hydrogen chloride and oxygen are shown. These gases are used for substrate surface preparation prior to silicon nitride film growth which will be discussed in detail later. The reaction

chamber was made of quartz. The substrate wafers were heated by an rf induction system with a graphite susceptor precoated with silicon carbide. A nitrogen inlet was connected to the exhaust line so that the exhaust gas is diluted with a larger amount of nitrogen prior to its venting.

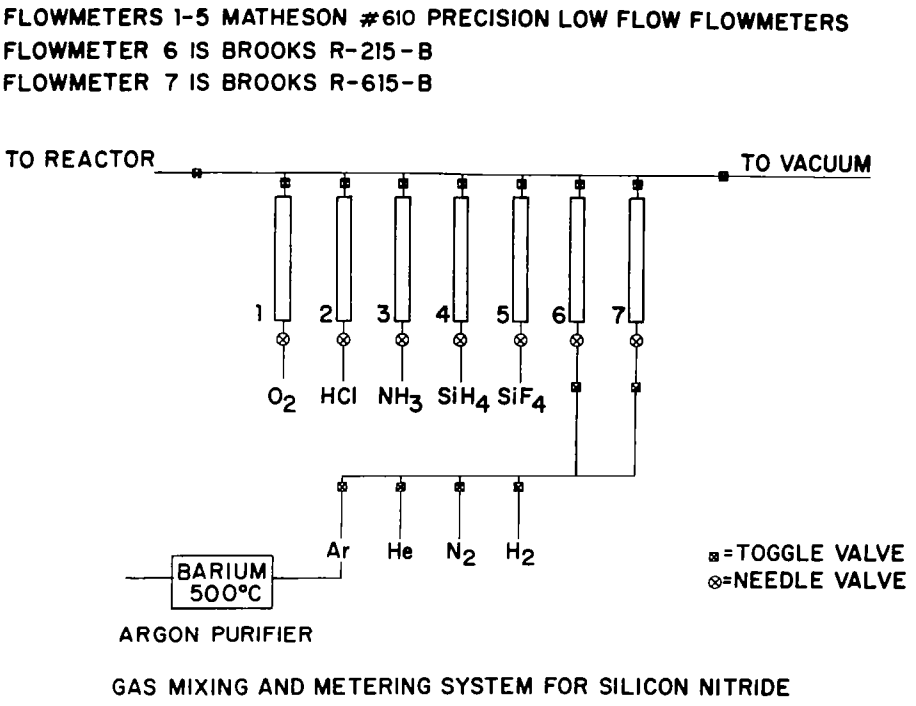


Fig. 1. Schematic sketch of the feed system.

The earlier reactors were made of round quartz tubing. The films grown in those reactors showed relatively large thickness variation from wafer to wafer and run to run. This was mainly due to unfavorable geometrical factors. Figure 2 shows the end view of the reactor. It is obvious that the susceptor can be laterally tilted toward either left or right side. Figure 3 shows the front view of the reactor. The susceptor is intentionally tilted longitudinally to give a more uniform film growth along the longitudinal direction. Figure 4 shows the section view along the longitudinal axis of the graphite susceptor. The lateral spacing between the graphite susceptor and the reactor is the largest at the mid-section and the smallest at the end. This continuous change in spacing causes undesirable gas flow patterns. To optimize the reactor geometry, a rectangular cross-section reactor which was designed for uniform silicon epitaxial growth was used in the later part of this inves-

tigation. Figures 2-4 show that most disadvantages of the round reactor disappear in the rectangular reactor. However, there is one distinct shortcoming in the rectangular reactor; it can not be evacuated. By suitable purging, the residual air can be removed. Figure 5 shows the rectangular reactor used in this investigation. The silicon nitride films grown on one-inch diameter substrates in this reactor with a large flowrate of nitrogen carrier gas showed wafer to wafer thickness variation (for 1000 Å films) of about $\pm$7% and run to run variation of about $\pm$10%. This is a factor of 2 improvement as compared with the round reactor at small flowrate of hydrogen carrier gas.

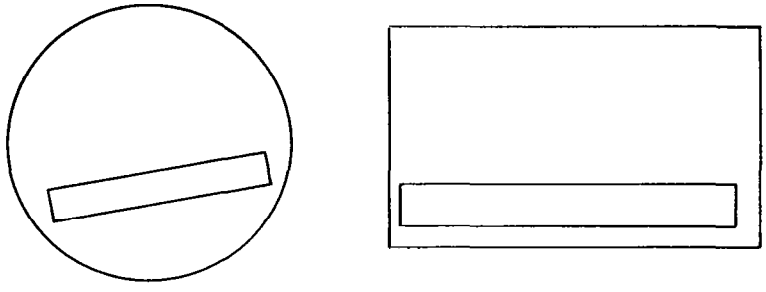


Fig. 2. End view of the round and rectangular reactors.

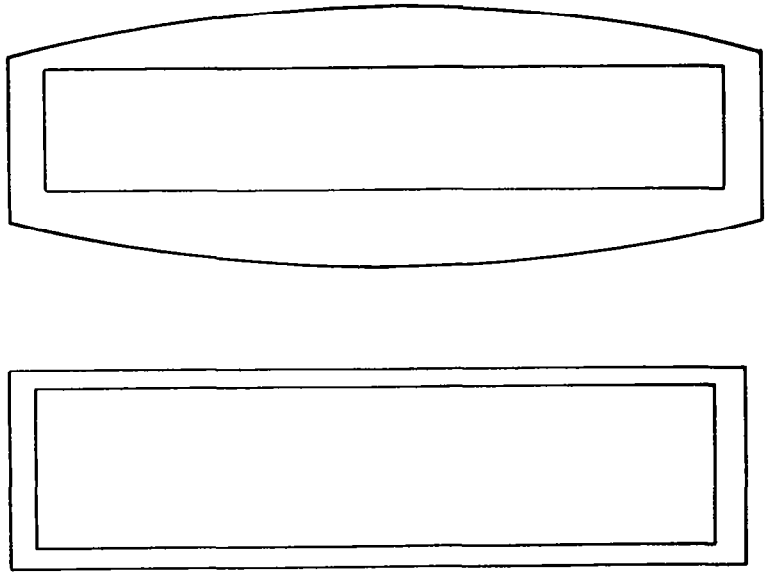


Fig. 3. Side view of the round and rectangular reactors.

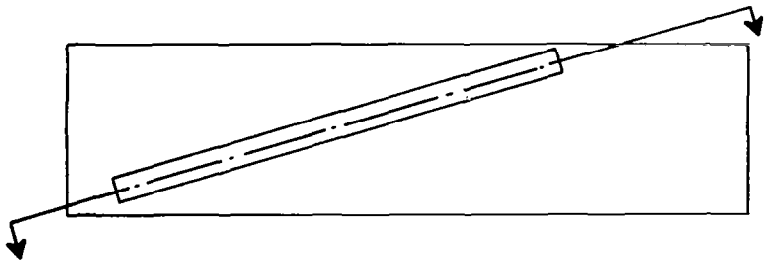


Fig. 4. Section view of the round and rectangular reactors.

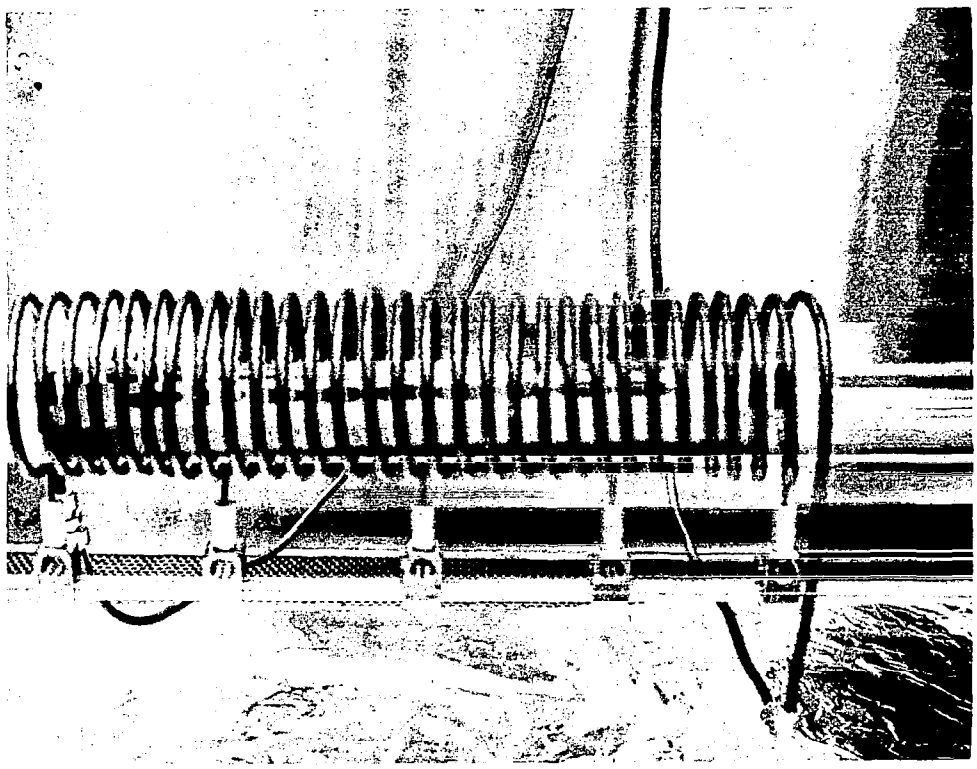


Fig. 5. Reactor in use.

The film thickness of the amorphous silicon nitride was measured at a step etched by hot H_3PO_4 [2] by the interference fringes under sodium light and checked by a Tolansky [3] interferometer. The index of refraction was determined by the differential interfringe spacing method [1] with sodium light (λ = 5900 Å) on samples which had the nitride films deposited on thermally oxidized silicon substrates. Estimated accuracy is ± 0.05.

Electrical properties of the films were investigated by means of MIS (metal-insulator-silicon) capacitors. After deposition of the silicon nitride films circular aluminum electrodes (20 mil diameter) were evaporated to form the MIS structures. Surface charge was determined from the well known capacitance-voltage measurement[4,5] using a frequency of 10 KHz or 100 KHz. Dielectric constant and electronic leakage measurements were made on the same structures.

1.2 SOURCE MATERIAL AND SUBSTRATES

The gases used in silicon nitride deposition are of high purity. The silane used for this work was supplied by Gray Chemical, Inc. The purity can be expressed in terms of the resistivity of the silicon epitaxy deposited on a single crystal silicon by the pyrolytic decomposition of silane. The Gray silane produced film resistivities greater than 50 ohm-cm. When the supply of Gray silane was exhausted, a cylinder of silane was supplied by Precision Gas Products, Inc. The Precision silane showed a resistivity of less than 5 ohm-cm. Another cylinder of Gray silane has been received later and the resistivity of its epitaxy is above 100 ohm-cm. Chromatographic analysis of ammonia has indicated that about 20 ppm air, within the instrumental sensitivity, is detected. The hydrogen gas was purified by a palladium-silver diffuser.

All substrate wafers used in this investigation were single crystal silicon unless otherwise specified. The substrate wafers were chemically polished. Prior to being loaded in the reactor, they were immersed in 10:1 buffered HF solution* followed by repeated rinsing in de-ionized water. The reactor is evacuated or flushed with N_2 prior to each run. To further clean the substrate, the wafers are subjected to either hydrogen chloride (about 1% in a hydrogen stream) vapor etch at 1175°C for 5 minutes or to heating in hydrogen at 1225°C for 10 minutes. In depositing alternate silicon nitride-silicon dioxide films, the silicon dioxide can be deposited either externally or in situ. When the first layer on the silicon substrate is oxide, it can be prepared by either thermal oxidation or by pyrolytic deposition from the reaction of silane (or silicon tetrachloride) and oxygen.

*10:1 buffered HF solution (10 parts 40% NH_4F and 1 part 48% HF).

1.3 NUCLEATION OF SILICON NITRIDE ON SILICON SUBSTRATES

The samples for nucleation study were grown under ordinary conditions except the growth time was shortened to the order of seconds. The first few samples were grown for 5 to 30 seconds with average growth rate (from prolonged runs) of about 20 Å per sec. To prepare the samples for transmission electron microscopic examination, the silicon substrate was thinned by the jet etch method.[6,7] Most samples had continuous silicon nitride films as detected by transmission electron diffraction and microscopic observation. The transmission electron diffraction pattern shows a typical diffuse ring, see Fig. 6, while the transmission electron micrograph is featureless because the silicon nitride is amorphous. The electron beam diameter was about 20-40μ. Electrical measurements confirmed the electron diffraction and microscopic observation that those films were continuous. This is in clear contrast with silicon nucleation on silicon substrates which showed isolated nuclei up to several hundred angstroms thick.

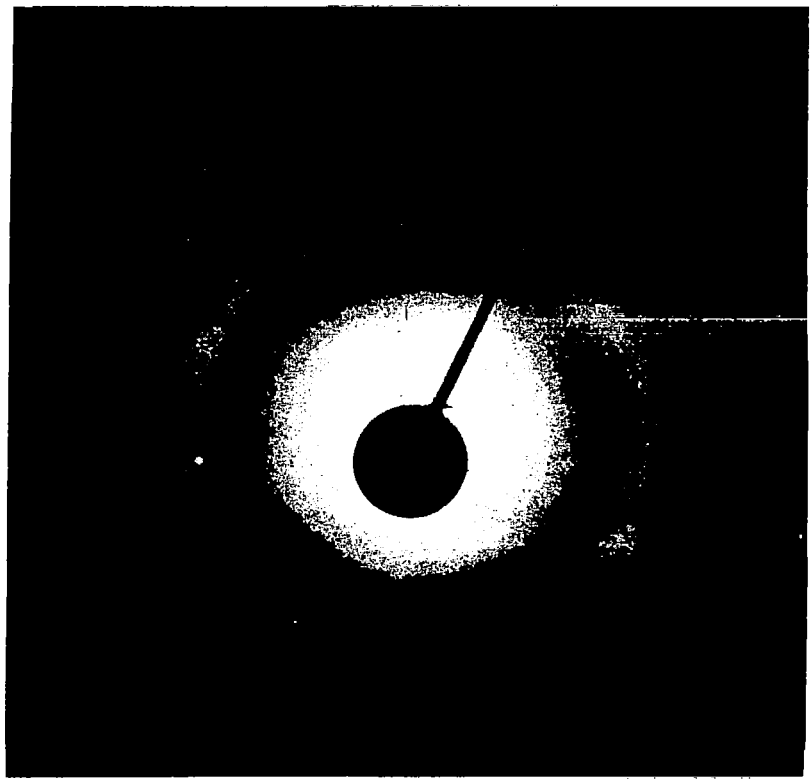


Fig. 6. Transmission electron diffraction pattern of amorphous silicon nitride films.

Two samples were grown with growth time of 1 and 3 sec., respectively. Again the silicon nitride films appeared to be continuous. It was thought that perhaps the reaction of NH_3 with the substrate produced a thin layer of silicon nitride, on which the nitride film quickly built-up through the SiH_4 - NH_3 reaction. A sample was heated in NH_3 for 2 min at the deposition temperature, 800°C. No trace of silicon nitride was detected. This indicates that either the silicon nitride film was so thin that the electron diffraction technique was not sufficiently sensitive to detect or no nitride was present. The results suggest that the silicon nitride nuclei formed primarily through the SiH_4 - NH_3 reaction rather than through nitriding.

In connection with uniform nucleation, it would be interesting to find the minimum thickness for pinhole free film growth. A simple electric method was used to detect pinholes in insulating film.[8] This method is quite similar to the electrolytic jet etch[6] with rock salt solution as the electrolyte. The method is simplified by using a drop of salt solution instead of continuous flow of salt solution as one electrode on dielectric film. Figure 7 shows a schematic sketch of the set-up for pinhole test. The results show that 3 second films are pinhole free while 1 second films may or may not be continuous. These results are in agreement with the transmission electron diffraction and microscopic observations.

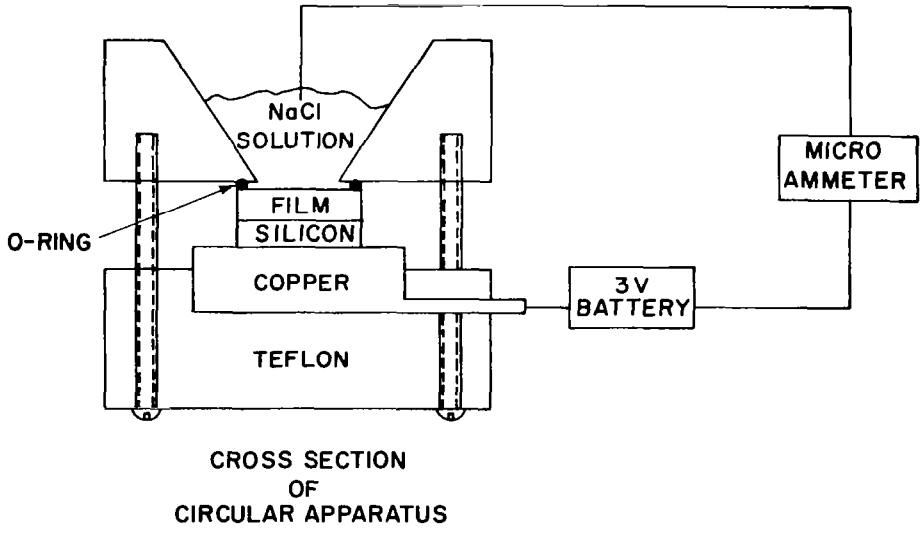


Fig. 7. Apparatus for electric measurement of dielectric defects in silicon nitride films.

1.4 SILICON NITRIDE GROWTH

1.4.1 In Hydrogen

Most of the pyrolytic silicon nitride films reported earlier[1] were prepared at the silane:ammonia ratio of 1:40 and some at 1:20. Within this range of silane:ammonia ratios, the growth rate and the physical properties of the films grown under equal conditions were essentially the same. When the ammonia fraction is gradually reduced, the composition of the films becomes silicon rich. Consequently, the film property changes accordingly.

The method of preparing pyrolytic silicon nitride has been reported elsewhere.[1] Silane and ammonia are used as the reactant gases. The reaction takes place in a quartz reaction chamber in which a constant flow of hydrogen as the carrier gas is maintained. The substrates are N-type silicon about 2.5 ohm-cm. After in situ cleaning by the method described above, the reactant gases in predetermined ratio are admitted into the reaction chamber. The silane:ammonia ratio varied from 1:1 to 1:10. The injection of silane and hydrogen is held at a constant rate throughout this investigation while the injection of ammonia is adjusted to the desired rate.

The growth rate of the silicon nitride film as a function of the reactant composition is shown in Fig. 8. The growth rate at a given temperature is practically independent of the ammonia injection rate with the SiH_4:NH_3 ratios of 1:1 to 1:10. The scattering of results was caused mainly by experimental error in controlling the low injection rate of reactant gases.

1.4.2 In Nitrogen

Nitrogen was used to replace hydrogen as the carrier gas in the later part of this investigation as stated in Section 1.0. The inlet gas flowrates are 1, 20 and 3×10^4 ml/min for silane, ammonia and nitrogen, respectively. The silicon nitride film growth rate is plotted against inverse temperature as shown in Fig. 9. Note that the growth rate at temperatures above $800^{\circ}C$ increases slightly with temperature up to $1000^{\circ}C$ while between $650-750^{\circ}C$, it increases rapidly with temperature.

A series of runs was made with film thickness as a function of deposition time. The growth parameters and the results are shown in Fig. 10. The results clearly show that the deposition rate is fairly constant from run to run.

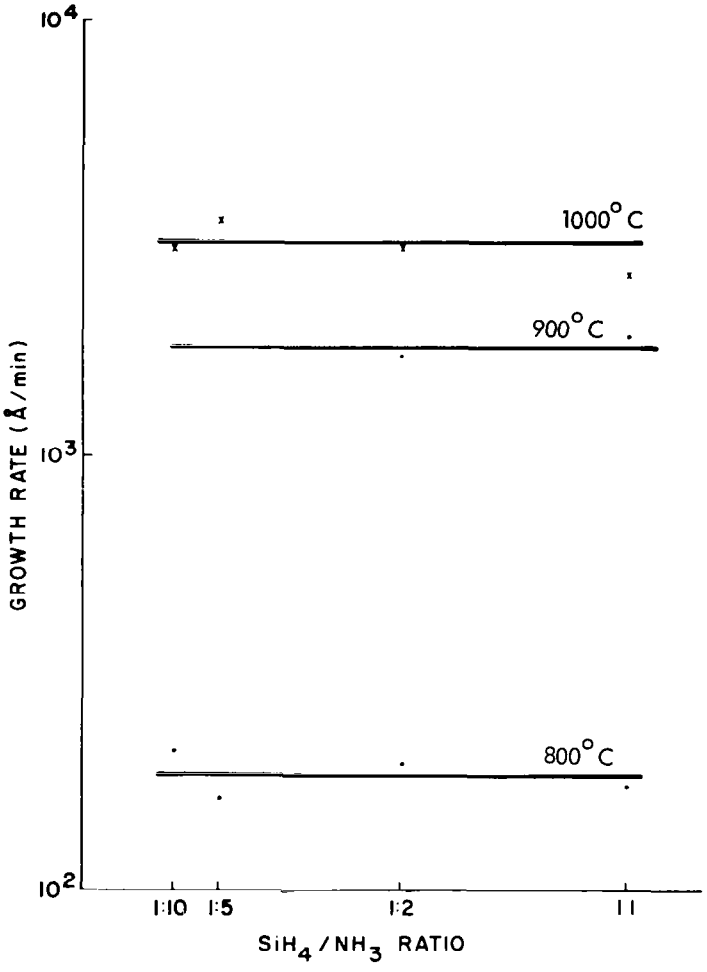


Fig. 8. Growth rate vs. SiH_4:NH_3 ratio carrier gas H_2.

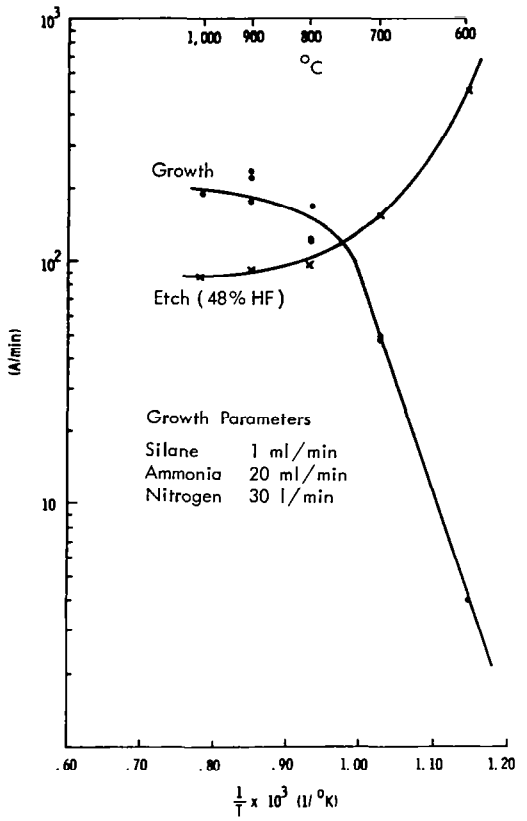


Fig. 9. Growth rate vs. temperature and etch rate vs. temperature.

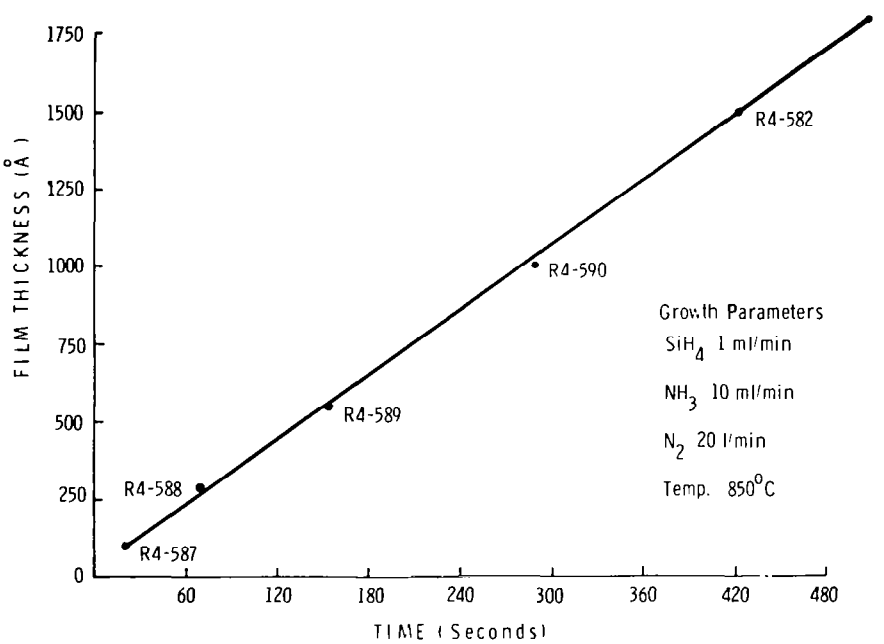


Fig. 10. Film thickness vs. growth time.

1.4.3 In Helium and Argon

Limited investigation has been made in using helium and argon carrier gases for silicon nitride film deposition. Because the molecular weight of He is much smaller than either SiH_4 or NH_3, the inlet gases in the reactor are rather inhomogeneous. Consequently the film thickness variation is large. Since bottled helium lasts only a few runs because a large flowrate is required, it is not practical for use as a carrier gas. However, it is interesting to note that the electrical properties of the film grown in helium are superior to that grown in any other carrier gases as will be described in later sections.

High purity argon is difficult to get. Argon was purified by passing through a hot barium bed.[8] For the large flowrate used in the reactor a purifier of substantial size would have to be designed and constructed. A few runs at relatively low flowrate were made and the electric properties on MNS (metal-nitride-silicon) were measured. The results which will be presented in later section indicate the films grown in argon are inferior to those grown in nitrogen or helium.

1.5 FILM STRUCTURE

1.5.1 Amorphous Films

The film structure of pyrolytic silicon nitride has been investigated by transmission electron diffraction and microscopy. The diffraction patterns of the silicon nitride films grown at SiH_4:NH_3 ratios within 1:1 to 1:10 have a typical diffuse ring for amorphous silicon nitride as shown in Fig. 6. The transmission electron microscopy was featureless because the film is amorphous. In one sample grown at 800°C with a SiH_4:NH_3 ratio of 1:1, a thin layer of polycrystalline silicon near the film-substrate interface was observed as shown in Figs. 11 and 12. The polycrystalline silicon growth at the interface may have been caused by a sudden surge of silane at the beginning of injection. Other samples grown under the same conditions showed no evidence of the presence of polycrystalline silicon.

1.5.2 Crack Formation

Earlier work[1] reported that cracks are often observed on thick silicon nitride films ($> 1\mu$) grown on silicon substrates as shown in Fig. 13. The density of

cracks increases with increasing film thickness and growth rate (> 500 $\mathring{A}$ min^{-1}). As mentioned above, those films were grown with a SiH_4:NH_3 ratio of 1:40. When the ratio is changed from 1:1 to 1:10 range, the potential for crack formation is greatly reduced. No cracking was observed on 1.5μ thick films even though the growth rate was a factor of 2 or 3 greater than 500 $\mathring{A}$ min^{-1}. These results indicate that the composition of the reactant gases has a profound effect on the stress and strain in pyrolytic silicon nitride films.

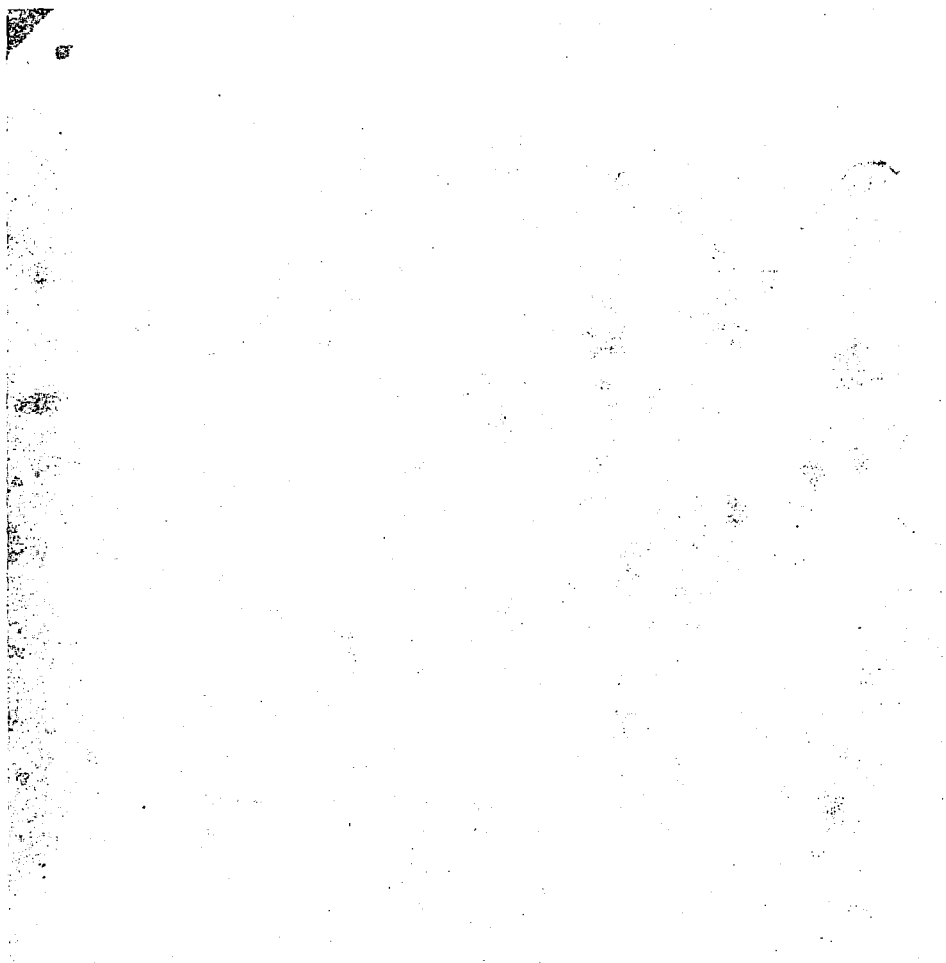


Fig. 11. Crystallites in 800°C film at Si_3N_4-Si interface detected by electron microscopy.

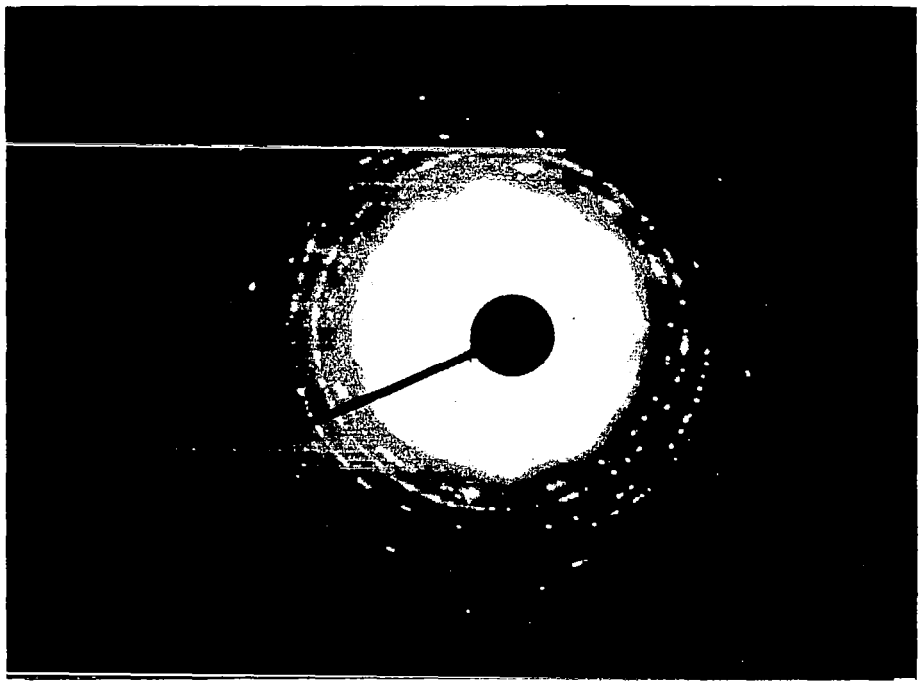
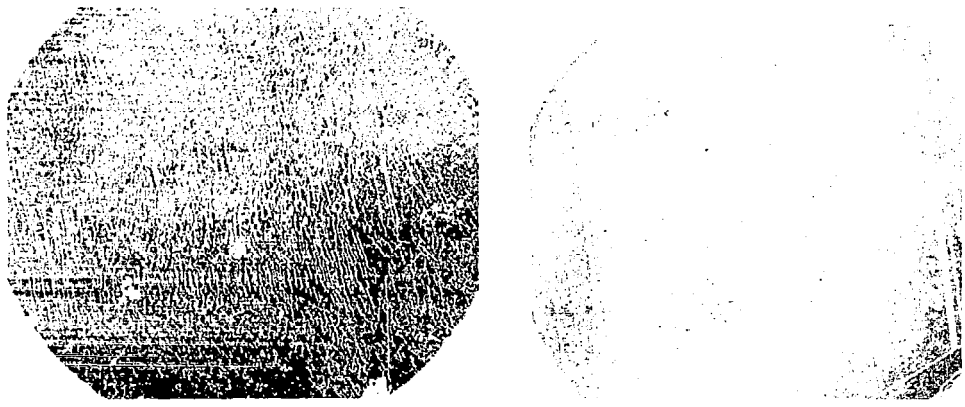


Fig. 12. The electron diffraction pattern of the same sample in Fig. 11.



(a) R4-103-4 As-GROWN CRACKS GROWTH RATE = 1200 Å/MIN

(b) R4-26 CRACKS DEVELOPED DURING ANNEALING IN H_2-HCl (1%) ATMOSPHERE AT 1350°C FOR 3 MIN

Fig. 13. Cracks in silicon nitride films.

1.5.3 Crystalline Silicon Nitride

Needle-crystallites were often observed on silicon substrates during high temperature deposition.[1] Recently, it was found that needle-crystallites were also formed on silicon substrates by vapor transport from the hot susceptor on which silicon nitride had accumulated in previous runs. During the in-situ surface cleaning, the substrates were heated at about 1250°C and the susceptor to about 1300°C. During this heating silicon nitride was transported from susceptor to substrate. The silicon nitride was in the form of needle-crystallites which were in clusters as shown in Fig. 14A. The needle-crystallites in each cluster have the same "root" which acted as the preferred nucleation site. X-ray diffraction study has identified the crystallites as α-Si_3N_4 (see Fig. 14B). The crystallites are extremely inert chemically. After being immersed in 48% HF for 48 hours, no evidence of etching was detected.

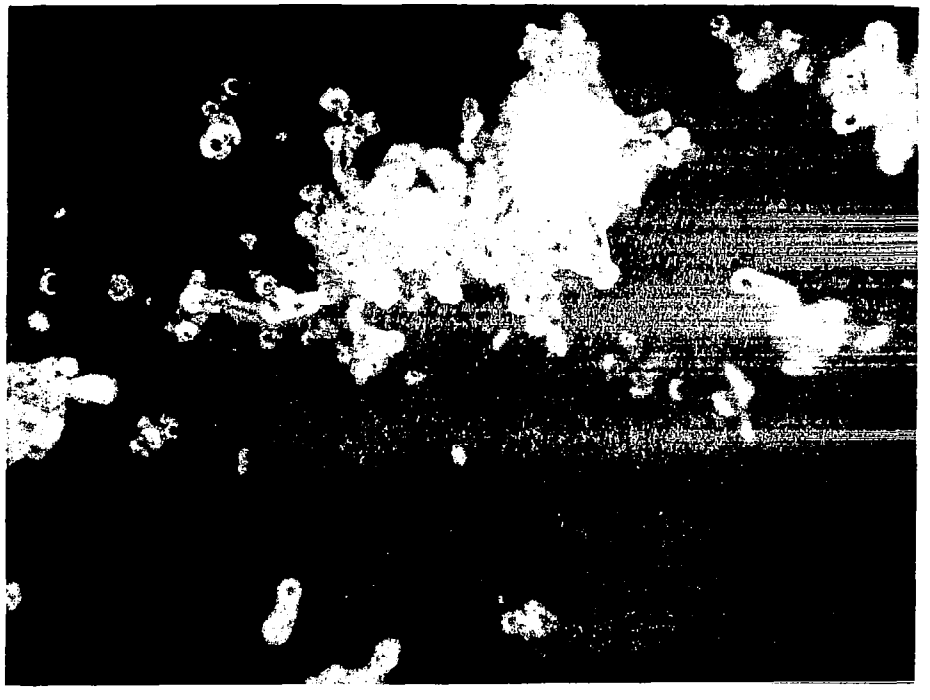


Fig. 14A. α-Si_3N_4 crystals on amorphous Si_3N_4 films.

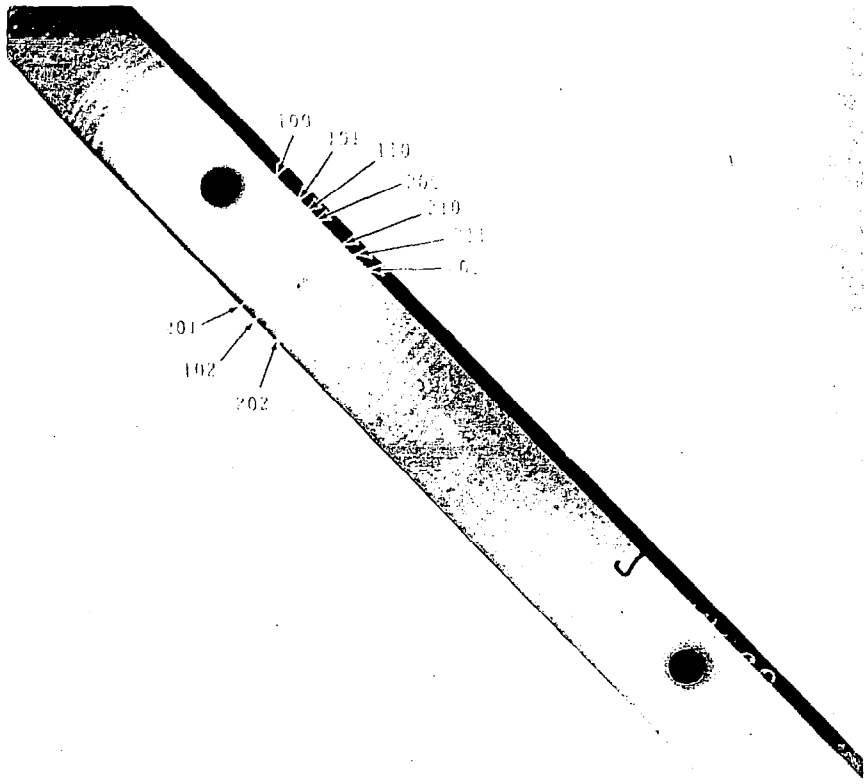


Fig. 14B. X-ray diffraction pattern of the α -Si_3N_4 crystals.

1.5.4 Composition Analysis

An attempt has been made to determine the silicon and nitrogen content in the silicon nitride films. Samples of the order of 1-10 mg of crystalline Si_3N_4 were analyzed spectrophotometrically for silicon and nitrogen. Spectrophotometric methods are usually accurate to 2-3% of the amount present.

The silicon analysis involved colorimetric determination of the silico-molybdate complex formed when silicon combines with molybdate in weak acid solutions. The nitrogen analysis involved removal of the nitrogen from Si_3N_4 by an alkali fusion collection, and determination colorimetrically using a modified Nessler-Jaackson reagent.

Of the two methods tried, the silicon seems to be the most feasible of the two if only one analysis is required. Further development of the nitrogen determination is required to improve its accuracy and reproducibility.

The results on analyzing crystalline silicon nitride are:

% Si from perchloric dehydration[9]	57.7 ±1% Si
% Si from silicon molybdate	58.5 ±3% Si
% Si theoretical	60.08%

The relatively large uncertainty in analysis accuracy leads to doubt if the techniques are meant to determine slight deviation from the stoichiometric composition. However, the analysis indicates that the crystal composition is closer to Si_3N_4 than any other Si-N compounds.

1.6 EFFECT OF SUBSTRATE PREPARATION ON SILICON NITRIDE GROWTH

In reviewing the electrical measurements on earlier samples as shown in Table I, it was noticed that all samples which were surface cleaned in situ by either hydrogen chloride vapor etch or by heating in hydrogen at or about 1200°C showed a relatively high flat band charge density, about $2.3 - 8 \times 10^{12}$ cm^{-2}. Several samples which had no in situ cleaning prior to nitride film growth, showed a surface charge density about $2.8 - 3.6 \times 10^{12}$ cm^{-2} which is consistently lower than those with in situ surface cleaning. The substrates without in situ surface cleaning are likely to have a thin layer of silicon dioxide. It is suspected that the presence of a few atomic layers of silicon dioxide on substrates prior to nitride film growth has helped to reduce the surface charge density. In order to find the effect of silicon dioxide on surface charge density, several samples were coated with either thermal or pyrolytic silicon dioxide (~450 - 470 Å) before being loaded into the reactor for nitride growth. The resultant surface charge density was reduced by a factor of 2, $\sim 1.5 \times 10^{12}$ cm^{-2}. The growth rate of silicon nitride on amorphous silicon dioxide substrates is comparable to that on silicon substrates under the same growth conditions.

Because the presence of silicon dioxide on silicon substrates prior to silicon nitride deposition improved the surface property of silicon, it is desirable to investigate the effect of the oxide thickness and method of preparing the oxide on the surface property of silicon. Defects in deposited films often originate from

inadequate substrate surface preparation. Externally prepared silicon dioxide is easily contaminated during its exposure to room atmosphere. The presence of room dust on an oxide substrate causes discontinuities in subsequently deposited nitride films.

In situ surface cleaning of silicon substrate followed by in situ oxidation should provide an extremely clean substrate surface for nitride deposition. The feed system has been modified to accommodate the required gases for in situ surface cleaning and oxidation.

Earlier MOS measurements at the IBM Laboratory on pyrolytic oxide indicate that the surface charge density is about one order of magnitude higher than the thermal oxide. Therefore it is highly desirable to prepare in situ thermal oxide for the MNOS (metal-nitride-oxide-silicon) samples. The required oxide thickness ranges from 150 - 450 Å. The oxidation rate of such thin films is to our knowledge not available in literature. A series of oxidation runs were made in our reactor at 1000°C. Within the measurement error, it appears that the results deviate from the Evitts, et al. thickness-time plot in their Fig. 2.[10] However, when the oxygen is maintained during heating and cooling as well as at 1000°C, the result is a continuation of Evitts, et al. thickness-time plot as shown in Fig. 15.

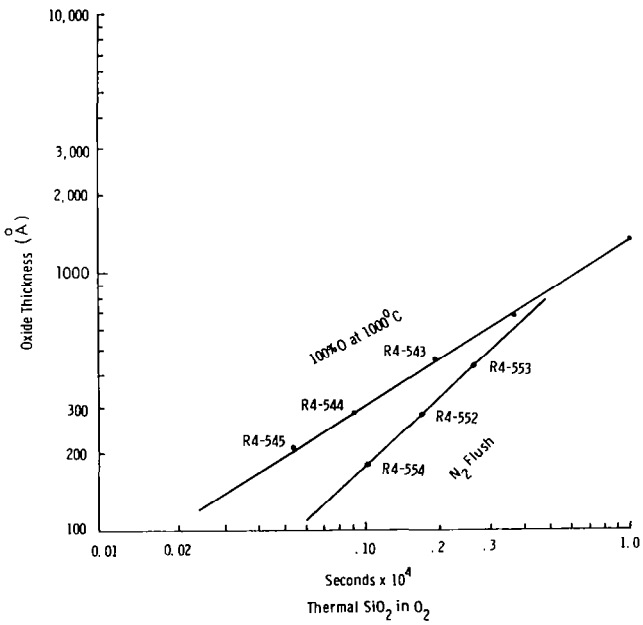


Fig. 15. SiO_2 thickness vs. oxidation time for thin oxides.

1.7 SILICON OXYNITRIDE GROWTH

The growth of silicon oxynitride films has been investigated. Thermodynamic analysis indicates that in the SiH_4-O_2-NH_3 system, oxide formation is favored at the temperatures up to 1250°C. Figure 16 shows the standard free energy change with respect to temperature.

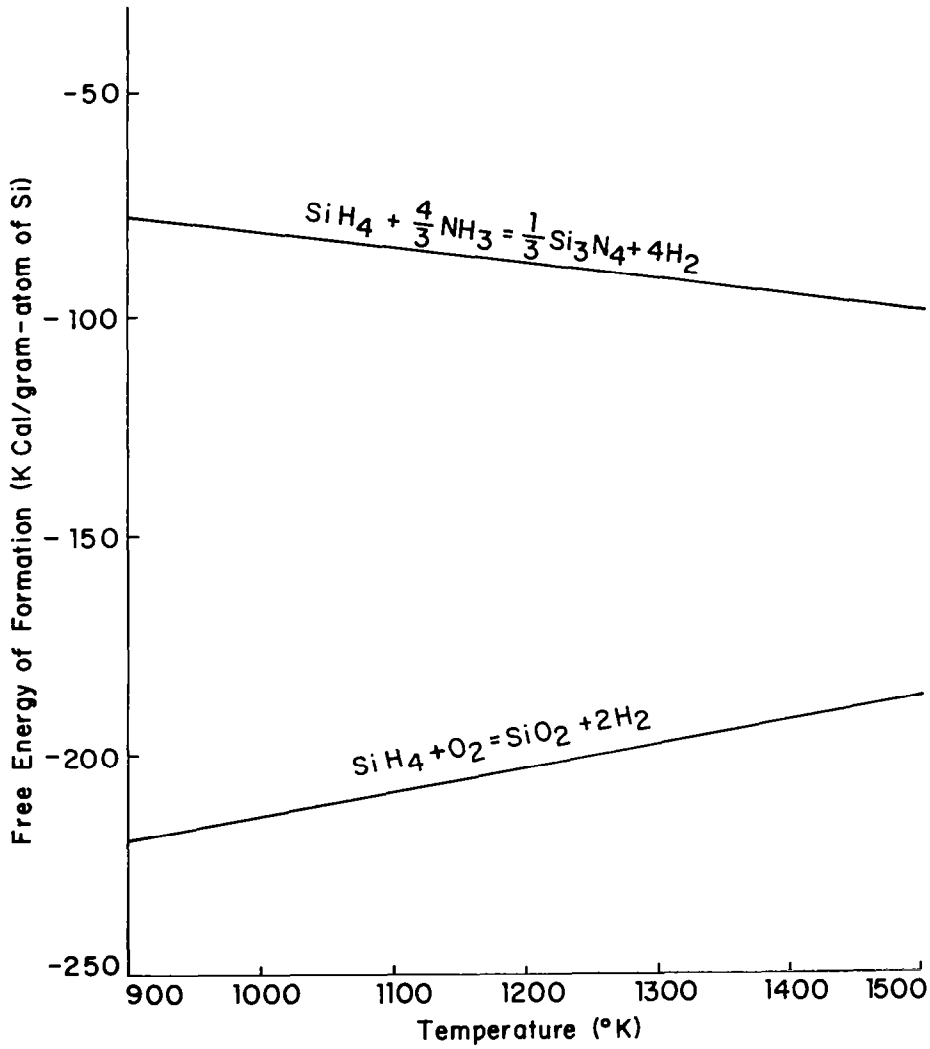


Fig. 16. Standard free energy vs. temperature.

The growth rate of the silicon oxynitride was investigated as a function of temperature. The growth parameters are: SiH_4 1 ml/min, NH_3 20 ml/min, O_2 0.5 ml/min and the carrier gas N_2 30 l/min. The growth rate vs. inverse temperature plot is shown in Fig. 17. Below 800°C the growth rate increases exponentially with temperature and above 800°C, the growth rate increase slowed down.

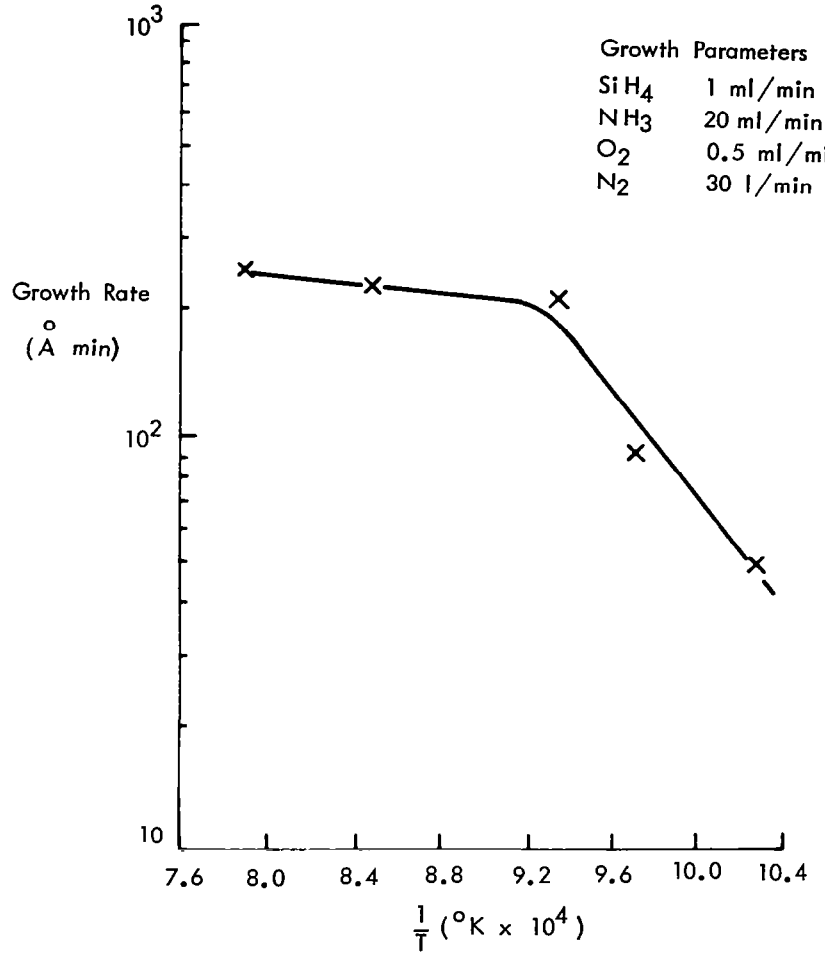


Fig. 17. Growth rate of silicon oxynitride vs. temperature.

The growth rate of the silicon oxynitride was also investigated as a function of oxygen injection rate. The growth parameters and the results are shown in Fig. 18. Note the sharp growth rate increase below 2 ml/min oxygen flowrate, above which up to 4 ml/min the growth rate remains essentially constant.

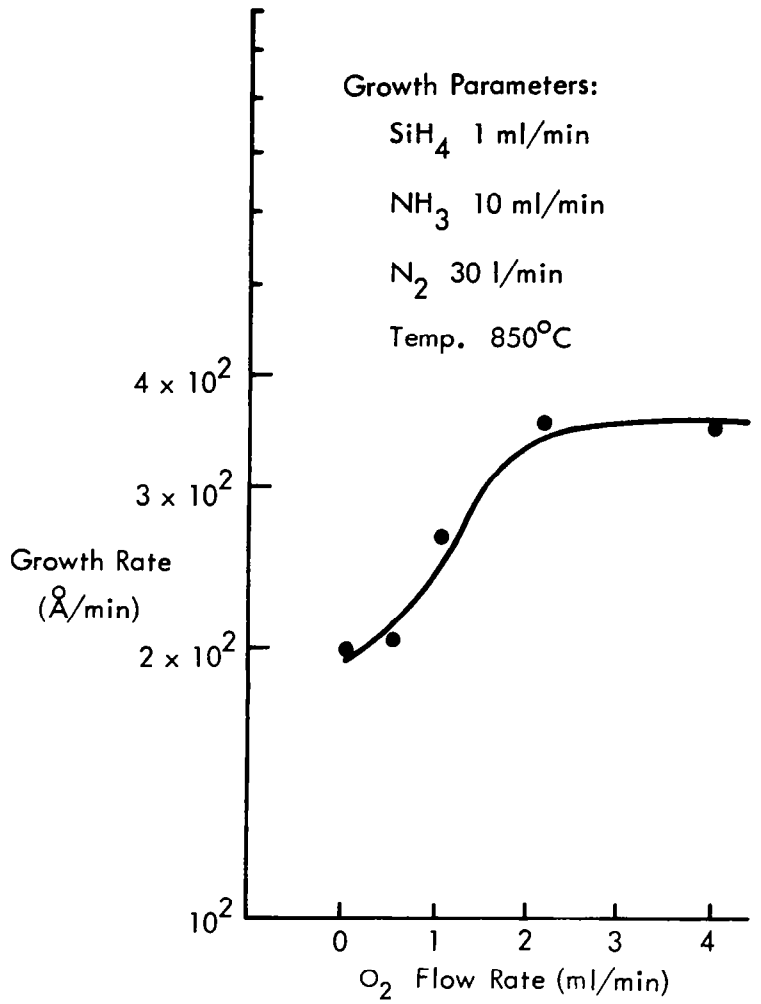


Fig. 18. Growth rate of silicon oxynitride vs. O_2 flowrate.

The structure of the silicon oxynitride films has been examined by using the electron diffraction and microscopy. None showed any trace of the presence of crystalline material.

The masking effect of the silicon oxynitride was briefly investigated. All the films (about 800 Å thick) which have etch rate of 180 Å/min or smaller in ~5% HF buffer etch resisted steam oxidation at 1150°C for 30 min. When the film thickness was above 1200 Å, they resisted steam oxidation (at 1150°C for 30 min) even though their etch rate was 300-400 Å/min. All silicon oxynitride films resisted common silicon dopant (B, Ga, P, and As) diffusion.

1.8 FILM DEFECTS

Defects in dielectric films are mostly caused by poor substrate preparation. Most potential defect sites on substrates are originated at dust particles, cleaning solution residue, impurity aggregates, pits, mounds and scratches, among which the first two are by far the most important factors. The impurity aggregates in substrates are formed in crystal growth and/or subsequent heat-treatment. Pits, mounds and scratches are caused by inadequate wafer polishing and handling, whereas dust particles and cleaning solution residues result from insufficient cleaning.

Scratch, pit and mound-free substrates can be prepared by the chemical-mechanical polish.[11] The dust particles and the cleaning solution residue demand careful surface cleaning prior to loading into the reactor. Several cleaning processes have been investigated. The best cleaning processes involve degreasing, repeated deionized water rinsing, acid etching, and again deionized water rinsing.

Several methods are available to detect defects in dielectric films. Chemical etch and electrical bias on MOS samples[12] are destructive methods. The leakage current measurement method[7] is nondestructive but it does not show the defect locations. Electrophoretical decoration method[13,14] is nondestructive and simple to use. Most of our investigations on film defect density were made by means of the electrophoretic decoration method.

The results indicate that by using suitable surface cleaning processes, the defect density can be reduced down to about 50 per cm^2. Impurity aggregates and scratches are important defect nucleation sites. Figure 19 shows the substrate surface defects caused by the solution growth[15] occurring during epitaxial silicon deposition on a substrate on which trace of gold was left behind from the gold plated tweezers. Apparently, during the solution growth, the molten solution moved and left tracks on wafers surface.

Figure 20 shows the decorated film defects at the tail of surface tracks. After the silicon nitride film was etched away, the sample was etched in Sirtl etch and the result is shown in Fig. 21. The etch pits were located at exactly the same spots where the decorated film defects were observed. The etch pits were formed by

the preferred etch at the impurity aggregates. Figure 22 shows the decorated film defects along the scratches. Before decoration, the scratches are not visible under a microscope. It is noted that stacking faults and dislocations do not seem to act as the film defect sites.

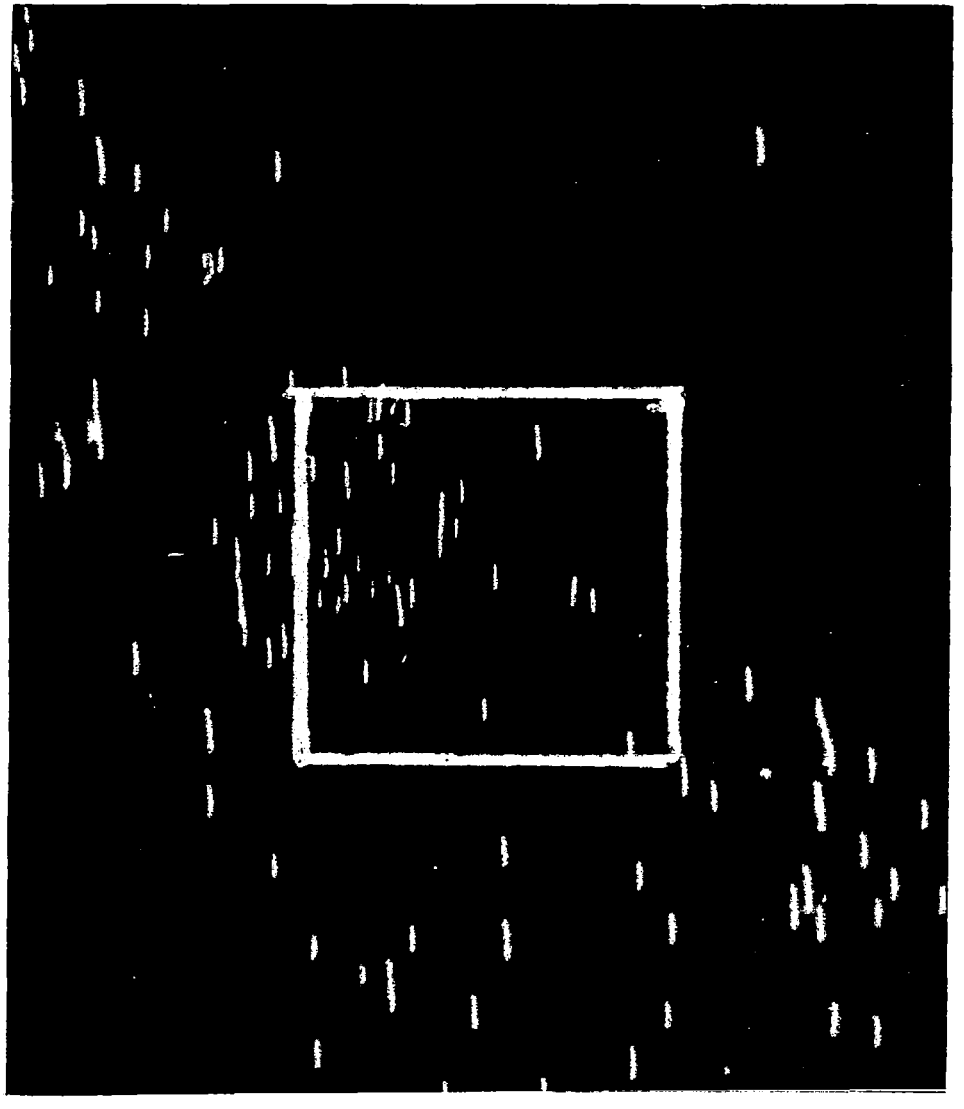


Fig. 19. Surface defects on substrate.

Fig. 20. Decorated defects in silicon nitride film.

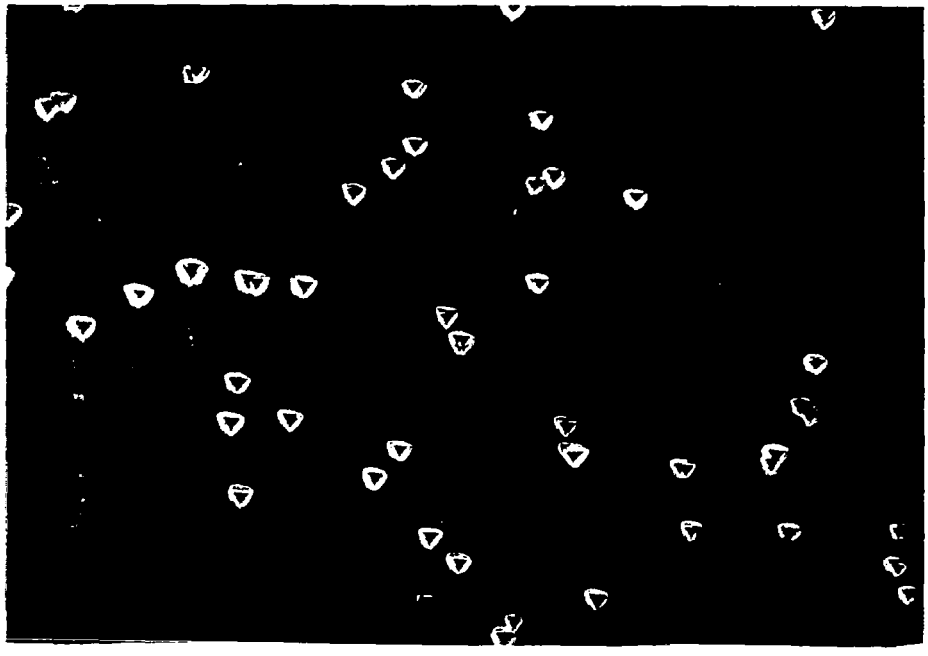


Fig. 21. Etch pits at the impurity aggregates.

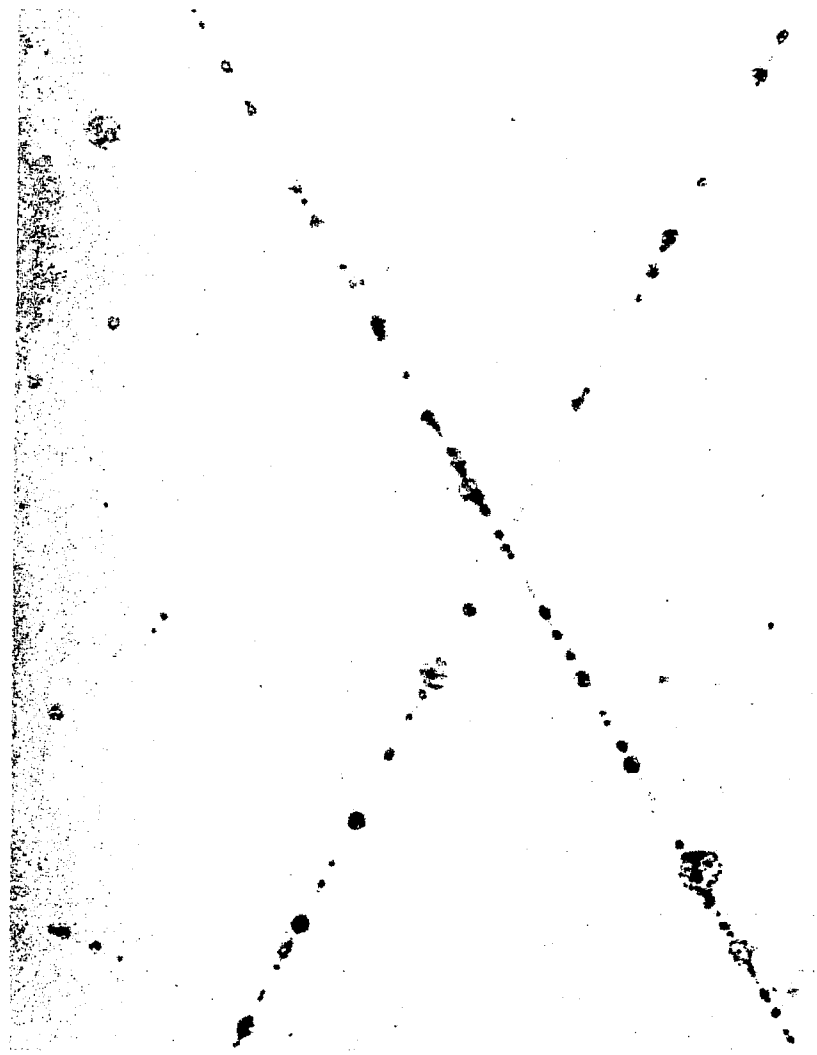


Fig. 22. Film defect along scratches.

Silicon nitride films which have been thinned down by chemical etch showed higher defect density than the as grown films of the same thickness. In other words, chemical etch introduces defects into the film. A similar effect has been observed in silicon dioxide.[11,13]

2.0 FILM PROPERTIES

The optical, electrical and chemical etching properties of silicon nitride were investigated. The electrical properties investigated include: the surface charge, stability, dielectric constant and electronic conduction.

2.1 INDEX OF REFRACTION

The index of refraction of a dielectric film is to a certain extent indicative of its density (or porosity) and its composition. The measured refractive indexes of silicon nitride films grown in hydrogen or nitrogen carrier gas and of silicon oxynitride films are presented below.

2.1.1 Silicon Nitride

The refractive index of the silicon nitride films grown in hydrogen carrier gas has been investigated as a function of silane to ammonia ratio. Figure 23 shows the measured results. In general, the refractive index increases with decreasing ammonia injection rates at all the deposition temperatures (from 800°C to 1000°C). When the ammonia injection rate equals the silane injection rate, the refractive index of the amorphous silicon nitride films exceeds that of the crystalline α-silicon nitride ($\mu = 2.1$).[9] These results strongly suggest that the composition of the pyrolytically deposited films changes gradually toward silicon rich silicon nitride as the ammonia injection rate is reduced to approach the silane injection rate. Since the film structure is amorphous, the excess silicon atoms must be dispersed randomly within the silicon nitride.

It should also be noted that the refractive index is temperature dependent; i.e., decrease with temperature. This is conceivable because the film density is expected to change in the same direction.

Similar results have been observed in films grown in nitrogen.

2.1.2 Silicon Oxynitride

The refractive index of oxynitride appears very indicative of the oxide content in the film although the direct relation is not established because the actual film composition is not determined. Under constant reactant gas composition, thermodynamic data indicate that the reaction is increasing in favor of oxide formation as the temperature decreases. Therefore, one would expect to find the refractive index to decrease with decreasing temperature because the R.I. of oxide (~1.45) is lower than that of nitride (~2.00). The results shown in Fig. 24 are indeed as expected.

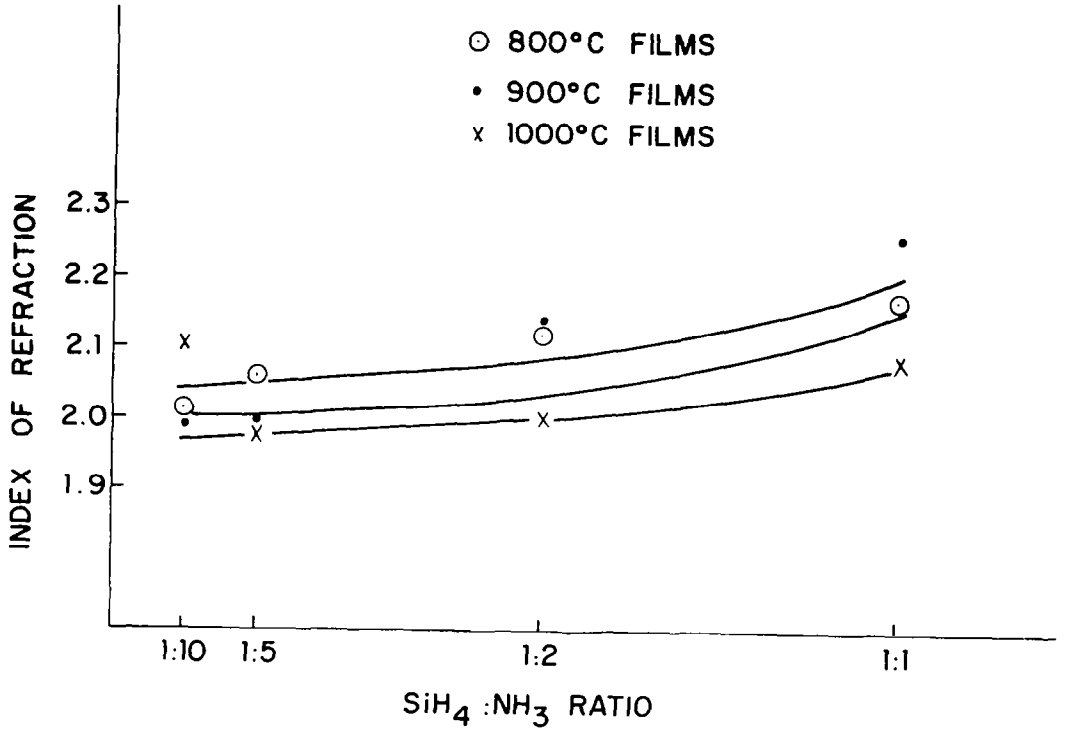


Fig. 23. Refractive index of silicon nitride vs. SiH_4:NH_3 ratio hydrogen grown films.

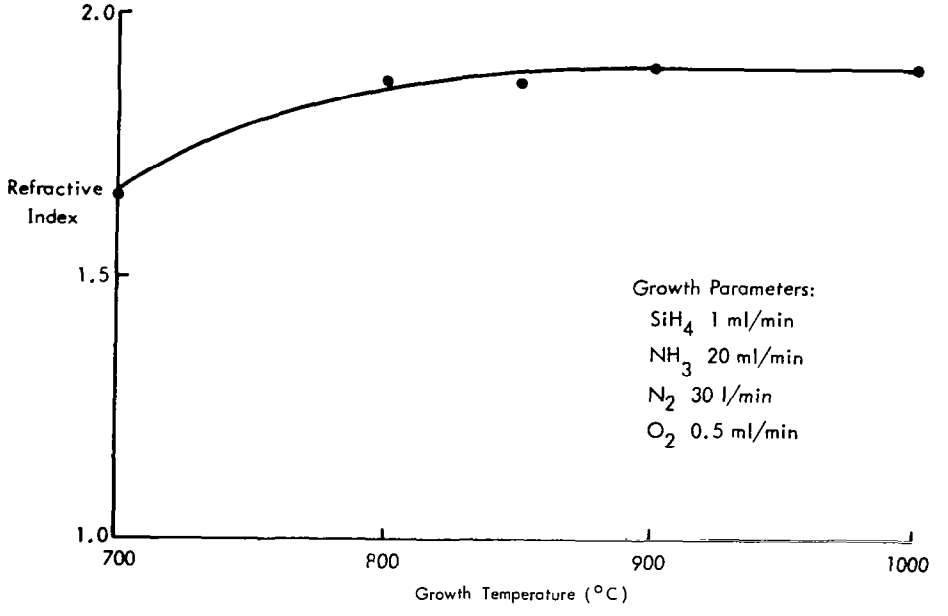


Fig. 24. Refractive index of silicon oxynitride vs. temperature.

It is further confirmed from the refractive index vs. oxygen flowrate plot as shown in Fig. 25. As the flowrate of oxygen increases while that of silane and ammonia are constant, the oxide content would obviously increase. Figure 25 shows the refractive index decreases as the oxygen flowrate increases. When the oxygen flowrate reaches 3 ml/min and higher while the silane and ammonia flowrate maintained at 1 and 10 ml/min respectively, the film composition was almost completely oxide.

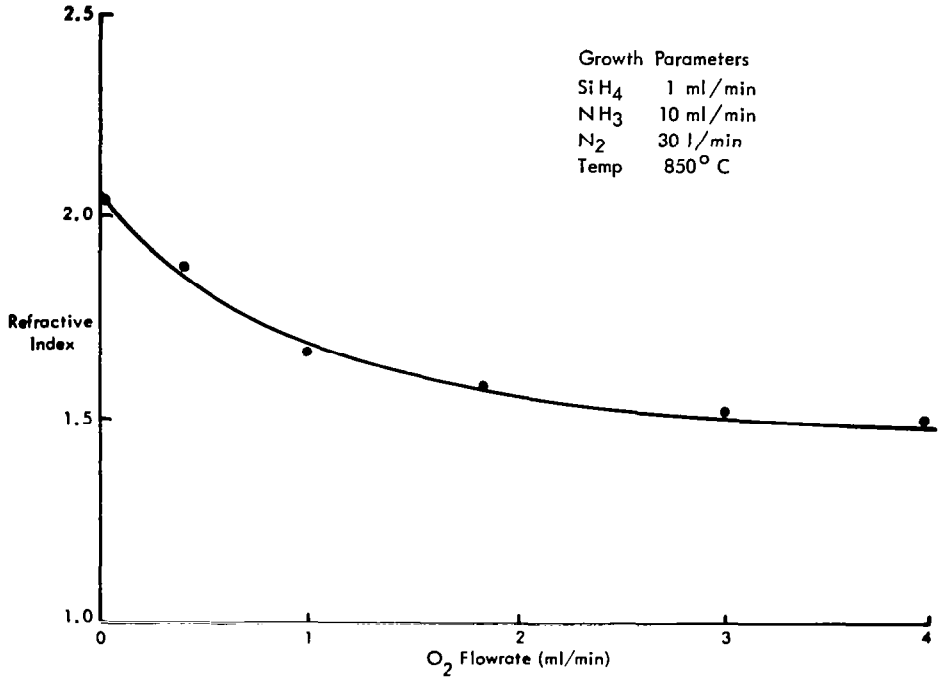


Fig. 25. Refractive index of silicon oxynitride vs. O_2 flowrate.

2.2 ETCH RATE

The etch rate of silicon nitride or oxynitride in HF solution is, like the refractive index, indicative of the film density (or porosity) and composition. 48% HF solution and 10:1 buffered HF solution were used to determine the etch rate of silicon nitride and oxynitride respectively. The etch rate of the former solution is about an order of magnitude greater than the latter.

2.2.1 Silicon Nitride

The etch rate is plotted as a function of the silane to ammonia ratio as shown in Fig. 26. The etch rate of the silicon nitride grown in hydrogen at a given silane to ammonia ratio decreases as expected with increasing deposition temperature because the film density should increase with temperature. The 800°C films dissolved much faster than the 900° and 1000°C films. The etch rate of the films grown at a given temperature decreases with decreasing ammonia injection rate as it approaches the silane injection rate. This could be due to the film composition changing toward the silicon rich silicon nitride.

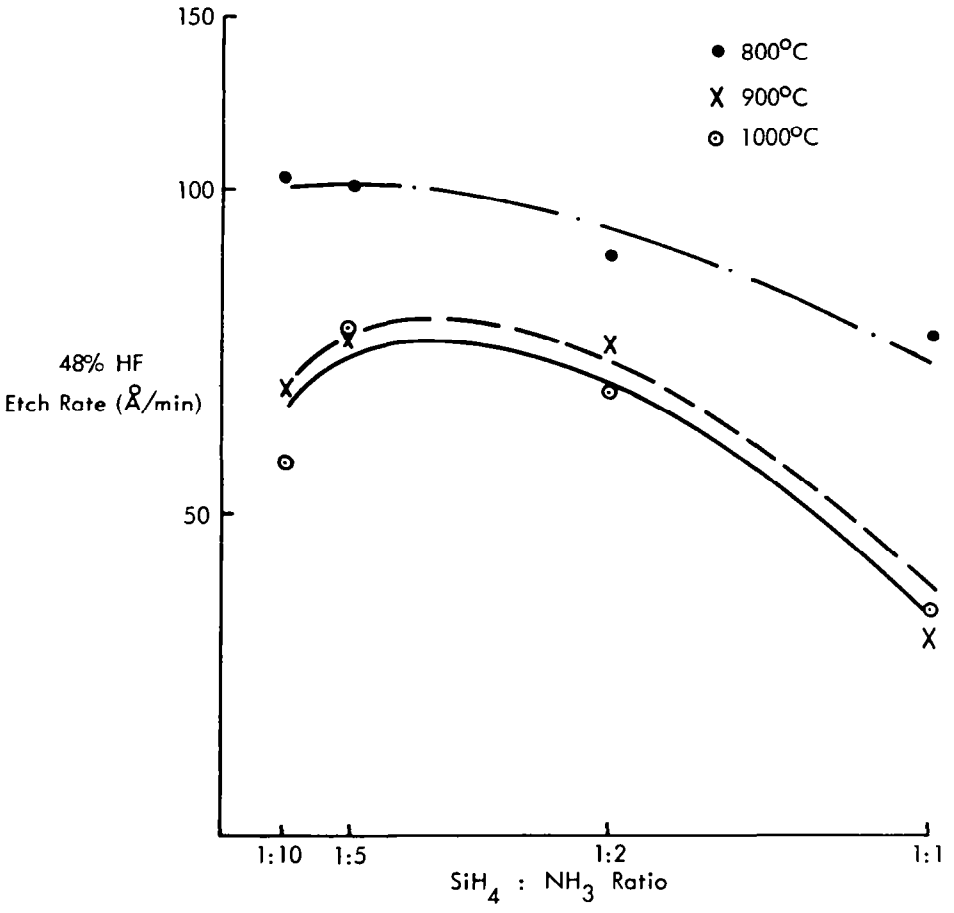


Fig. 26. Etch rate of silicon nitride in 48% HF vs. SiH_4:NH_3 ratio carrier gas H_2.

The etch rate of the silicon nitride films grown in nitrogen is plotted as a function of the growth temperature as shown in Fig. 9. In general, the etch rate increases with decreasing growth temperature. However, the change of the etch rate of the films grown above 800°C is much smaller than that grown below 800°C.

2.2.2 Silicon Oxynitride

The etch rate of silicon oxynitride in 7:1 buffered HF solution* was investigated as a function of substrate temperature and the oxygen flowrate during film growth. Figure 27 shows the etch rate vs. inverted temperature plot. This curve is quite similar to the etch rate curve in Fig. 9 for silicon nitride in 48% HF. The high temperature films etched slower, primarily due to higher density, than the low temperature films. The etch rate increase from 1000°C to 800°C is slower than from 800°C to 700°C which indicates that the film density change is more drastic in the temperature range of 700°C to 800°C than from 800°C to 1000°C.

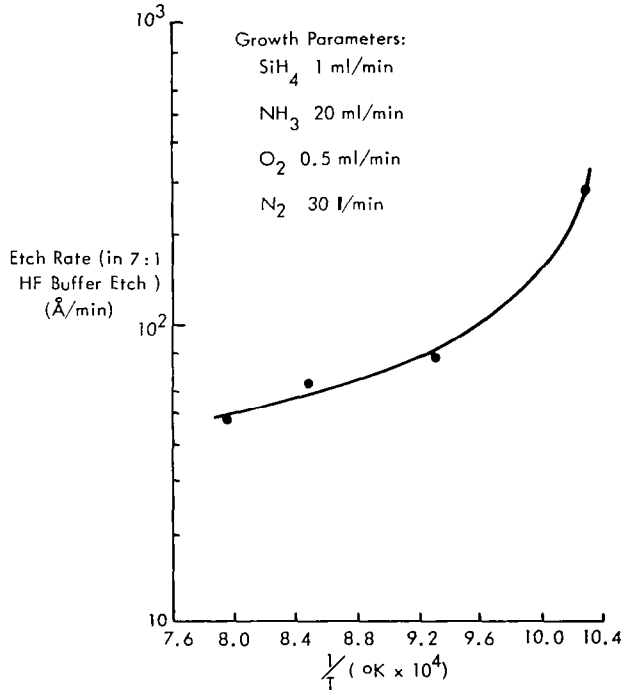


Fig. 27. Etch rate of silicon oxynitride in 7:1 buffered HF solution (7 parts 42% NH_4F and 1 part 50% HF) *vs. temperature.*

*7:1 buffered HF solution (7 parts 42% NH_4F and 1 part 50% HF).

The change of the etch rate as a function of oxygen flowrate during film growth is shown in Fig. 28. In this case the major change in films is the oxide content. The etch rate of the pure pyrolytic SiO_2 grown under the same conditions (850°C and ~3000Å/min) is about 2 orders of magnitude greater than the pure nitride. The silicon oxynitride which is more or less a mixture of oxide and nitride should have its etch rate increasing with increasing oxide content (or oxygen flowrate during growth). Figure 28 shows indeed that the etch rate increases rapidly with a small increase of oxide at the low oxide region. Then the rate of increase gradually reduced. When the films contain mostly oxide (at 3 ml/min O_2), the etch rate approaches its peak.

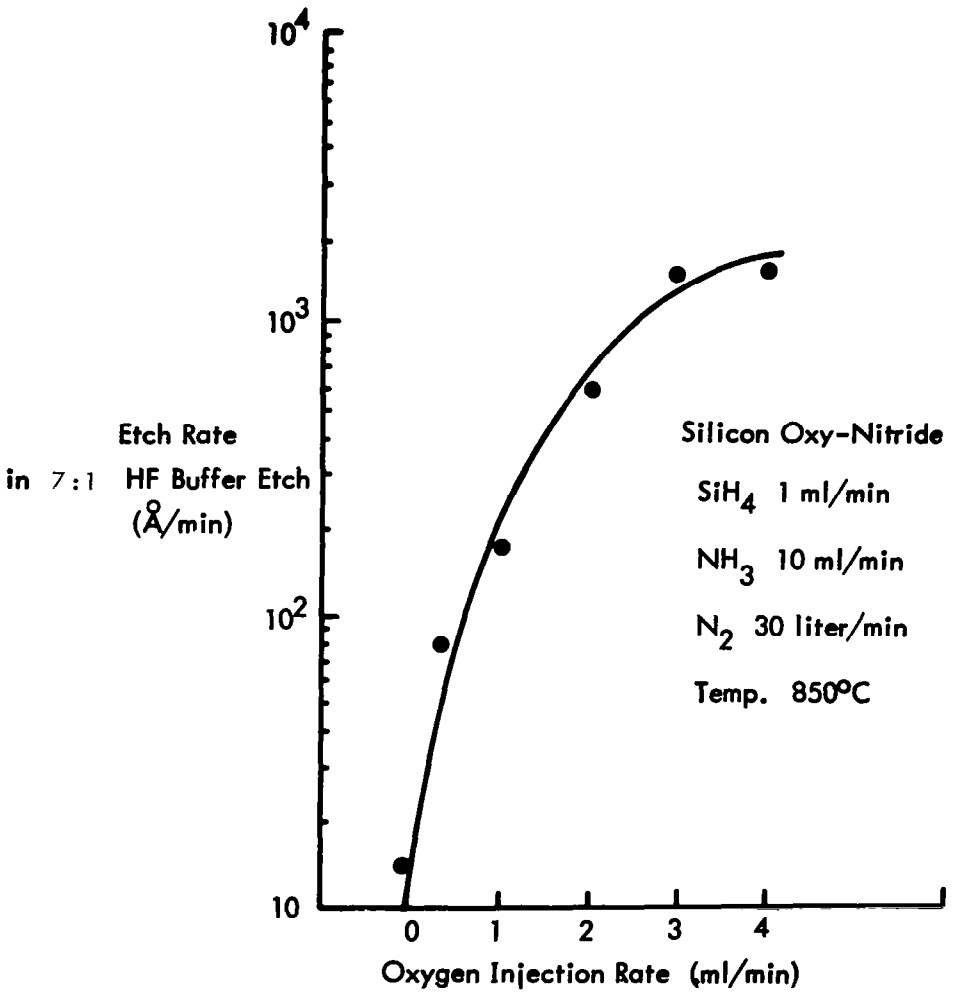


Fig. 28. Etch rate of silicon oxynitride in 7:1 buffered HF solution (7 parts 42% NH_4F and 1 part 50% HF) vs. O_2 flowrate.

2.3 ELECTRICAL MEASUREMENTS

Most electrical measurements on the silicon nitride films were obtained from metal-insulator-silicon (MIS) capacitors formed by evaporating circular aluminum electrodes (20 mil diameter) onto the deposited films. These devices have the obvious advantages of very simple fabrication and ease of measurement. In addition, a number of important interfacial and bulk film properties can be determined from this simple structure. If the film thickness is known, the dielectric constant and electric field strength are easily measured. Electronic conduction may be measured over a wide range of field strength and current density. A most important property is the sign and magnitude of surface charge at the insulator-silicon interface, which may be determined from a measurement of small-signal capacitance vs. dc bias (C-V measurement).[4,5] A good passivation insulator will produce a low surface charge when applied to the semiconductor of interest (silicon in the case of this study), and this surface charge will be stable during the operating life of the fabricated device. The stability of MIS devices is measured simply by comparing C-V traces before and after various stress treatments such as: electric field combined with elevated temperature, high field at room-temperature, or high temperature annealing in various ambients.

Figure 29 schematically shows typical C-V traces on n-type silicon and defines several symbols used in this report. A frequency in the range of 10 ~ 100 KHz is normally used for this measurement. The insulator capacitance is C_I (farads/cm^2), and this determines the maximum capacitance, occurring when the silicon surface is in accumulation (electron density greater than bulk density). As metal bias is swept in a negative direction, the silicon surface is depleted, and the series capacitance of the depletion layer causes a decrease in the overall capacitance. At more negative bias an inversion layer forms, and capacitance saturates at a minimum level. The flat-band capacitance C_{FB} is easily calculated[4] for any known C_I and silicon impurity concentration, and occurs when there is no energy-band bending in the silicon at the insulator-silicon interface. Flat-band bias V_{FB} is the measured bias for this condition, and surface charge N_{FB} is defined in Fig. 29 (having units of electronic charges/cm^2). The flat-band bias V_{FB} will be zero if there is no charge in interface states or insulator space charge. Positive charge in the insulator or surface states induces a negative surface charge in the silicon at zero bias, and V_{FB} will be negative. In the absence

of active surface states, N_{FB} is equal to the zero-bias Si surface charge in sign and magnitude. With surface states present, a portion of V_{FB} causes a charging (or discharging) of the states, and N_{FB} is somewhat larger than the zero-bias Si surface charge.

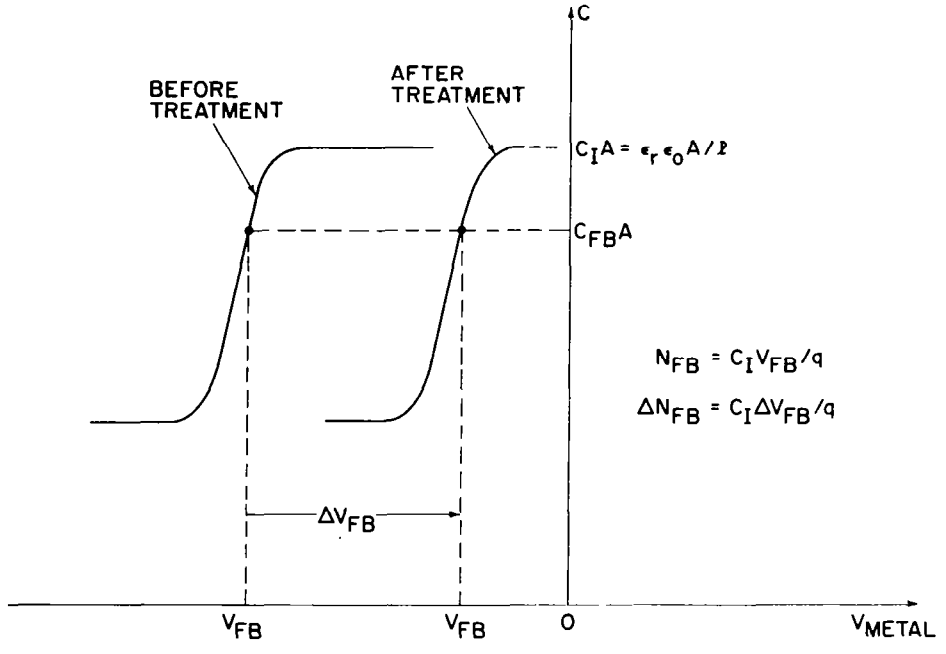


Fig. 29. Schematic MIS capacitance-voltage traces (on n-Si) defining terms used in describing such measurements. Note in this example that V_{FB} and N_{FB} values are negative while ΔV_{FB} and ΔN_{FB} are positive.

2.3.1 Surface Charge

A large number of measurements have been made to determine the effects of deposition parameters on flat-band surface charge, N_{FB}. The deposition parameters studied were: carrier gas (H_2, He, N_2, Ar), silane:ammonia ratio, deposition temperature, and surface preparation (including formation of SiO_2 prior to Si_3N_4). In general, N_{FB} shows no strong dependence on the thickness of a nitride film (V_{FB} is thus proportional to thickness) or on the silicon doping type or resistivity. Cleaning of the silicon surface before deposition is not critical, since samples without special cleaning gave the same N_{FB} as samples which had an in situ HCl vapor etch before silicon nitride deposition. The only surface treatment giving a clear reduction in N_{FB} was the formation of a thin SiO_2 layer before nitride deposition, and this will be discussed in detail later.

When pyrolytic silicon nitride is deposited on bare silicon a negative N_{FB} is found with a magnitude in the range of 1 to 6 x $10^{12}/cm^2$. This is the same sign but an order of magnitude larger N_{FB} than found with thermal SiO_2 on Si. The dependence of N_{FB} on carrier gas, deposition temperature, and silane:ammonia ratio is shown by data in Table 1. These films were deposited on n-type silicon of 1-2 ohm cm resistivity. Film thicknesses cover a wide range because of the range of deposition rates, but most are between 1000 Å and 10,000 Å. The wafers with H_2 carrier gas films were baked in H_2 at 1200°C before deposition. This was found to have no significant effect and was omitted in other runs, which had only a HF-HNO_3-HF rinse sequence before furnace loading and deposition. Films deposited

TABLE 1. Effects of Carrier Gas, Temperature, and Silane:Ammonia Ratio on N_{FB} for Si_3N_4 Deposited on Bare Silicon.

Wafer No.	Carrier Gas	Temp (°C)	SiH_4:NH_3 Ratio	$-N_{FB}$ ($10^{12}/cm^2$)
4160	H_2	800	1:1	3.3
4161			1:2	3.4
4165			1:5	3.8
4163			1:10	3.7
4050		870	1:40	2.3
4166		900	1:1	2.7
4167			1:2	2.8
4168			1:5	3.1
4169			1:10	2.8
4170		1000	1:1	4.8
4171			1:2	5.4
4172			1:5	5.1
4173			1:10	5.4
4280	He	800	1:1	1.2-3.0
4281			1:5	2.9
4282			1:10	3.5
4283			1:20	3.5
4284		900	1:1	2.3
4285			1:5	1.7
4286			1:10	1.8
4287			1:20	1.5
4288		1000	1:5	2.2
4290	N_2	700	1:10	6.6
4291			1:10	4.6
4292		800	1:5	3.9-5.0
4311			1:10	2.9
4293			1:20	3.7
4294		900	1:10	2.2
4295			1:20	1.4
4296		1000	1:1	2.7
4297			1:10	2.0
4298			1:20	0.8
4344	Ar	600	1:10	3.0
4345		700		6.8
4346		800		2.8
4347		900		2.2
4348		1000		2.1

in H_2 and He were measured at 10 KHz, and those deposited in N_2 and Ar were measured at 100 KHz. The results with each carrier gas can be summarized as follows: The data for hydrogen carrier gas are also plotted in Fig. 30. It is seen that N_{FB} with H_2 carrier depends on the deposition temperature, but shows very little dependence on the SiH_4:NH_3 ratio. The optimum temperature for minimum $-N_{FB}$ is near 900°C, but $-N_{FB}$ is always above 2 x $10^{12}/cm^2$. With He carrier we again see no strong dependence of N_{FB} on SiH_4:NH_3 ratio. The temperature dependence again indicates 900°C as an optimum temperature. The N_{FB} with 900°C films is about one-half as large as the N_{FB} with H_2 carrier at 900°C. The 1000°C data with He is limited because of an impractical deposition rate (< 50 Å/min). With N_2 carrier, $-N_{FB}$ decreases gradually as deposition temperature increases at a given SiH_4:NH_3 ratio. Also, for a given temperature, $-N_{FB}$ generally decreases with increasing ammonia fraction. The $-N_{FB}$ = 0.8 x $10^{12}/cm^2$ obtained with SiH_4:NH_3 = 1:20 at 1000°C is the lowest surface charge observed with nitride on bare silicon. With argon carrier, $-N_{FB}$ decreases slowly with increasing temperature. The dependence on SiH_4:NH_3 ratio was not investigated. The 700°C film data is anomalous since a broad C-V transition (fast states) was observed in addition to the high N_{FB}.

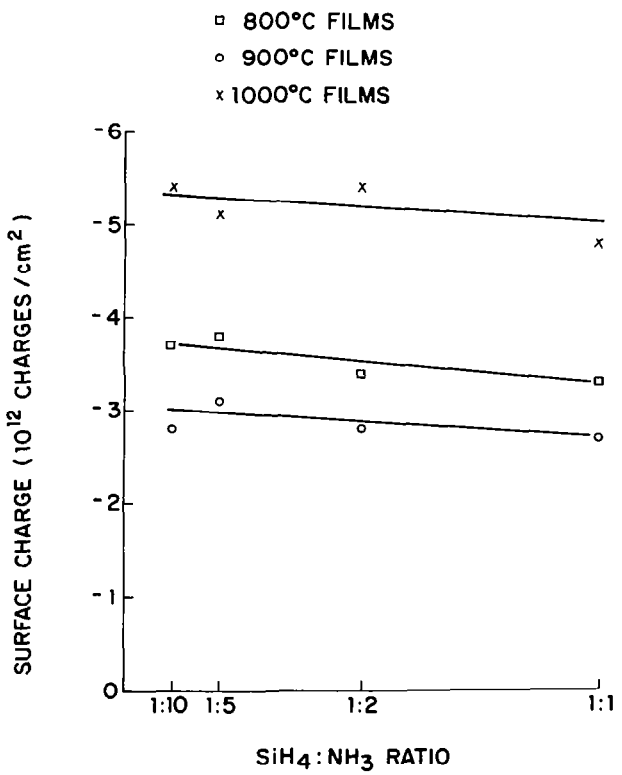


Fig. 30. N_{FB} vs. silane:ammonia ratio for pyrolytic silicon nitride films deposited on silicon in H_2 carrier gas. Measurement frequency is 10 KHz.

It was found that N_{FB} can be reduced if a thin layer of SiO_2 is formed on the Si before Si_3N_4 deposition. This also improves stability, which will be discussed in the next section. A number of experiments have been done with nitride-over-oxide structures to determine reproducibility of charge levels, influence of carrier gas, and dependence on oxide thickness. Table 2 gives the results of such an experiment comparing oxidized to non-oxidized wafers. Wafers of n-Si with and without a 450 Å thermal oxide were coated with pyrolytic silicon nitride in four runs under the same deposition conditions (He carrier, SiH_4:NH_3 = 1:10, 900°C). In some cases the oxide was stripped from half of a wafer before deposition. This resulted in N_{FB} as large as, or larger than, deposition on bare Si without any precleaning. Table 2 shows that deposition on oxide gives a reproducible, low N_{FB} whereas deposition on bare Si gives a large scatter in N_{FB} with values 2 to 6 times as large as the nitride-over-oxide case. A comparison of carrier gases for deposition over a 520 Å thermal oxide is shown in Table 3. All depositions were at 900°C with a SiH_4:NH_3 ratio of 1:10. These wafers were p-type Si (7 ohm cm), and the N_{FB} range over one wafer is shown in each case. Note that He carrier gave the lowest N_{FB} and H_2 the highest (the difference being within a factor of two). In all cases N_{FB} is improved over the value without SiO_2.

TABLE 2. N_{FB} from Several Runs with Nitride Deposited on Oxidized and Bare Silicon.

Deposition	No. of Runs	No. of Wafers	SiO_2 (Å)	$-N_{FB}$ ($10^{12}/cm^2$)
He, 900°C, SiH_4:NH_3 = 1:10	4	8	450	0.47 - 0.66
He, 900°C, SiH_4:NH_3 = 1:10	4	10	none	1.2 - 3.5

TABLE 3. N_{FB} of Nitride-Over-Oxide Structures for Various Carrier Gases.

Wafer	Oxide (A)	Nitride (A)	Carrier Gas	$-N_{FB}$ ($10^{12}/cm^2$)
4322	520	1590	H_2	1.4
4323		2980	He	0.7-0.8
4324		1640	N_2	0.9-1.3
4325		1950	Ar	0.8-1.1

Figure 31 shows the dependence of N_{FB} on oxide thickness for metal-nitride-oxide-silicon (MNOS) structures with three different oxide preparation methods. The three methods were: in-situ thermal oxidation (O_2, 1000°C) immediately prior to nitride deposition, thermal oxidation in another furnace (O_2, 1000°C), and in-situ pyrolytic deposition ($SiH_4 + O_2$, 750°C). About 1000 Å of nitride was deposited in all cases (860°C, N_2 carrier, SiH_4:NH_3 = 1:10 or 1:20). These data indicate that N_{FB} has very little dependence on oxide thickness for thicknesses of 150 Å and greater. Of the three oxidation methods tested, in-situ thermal oxidation results in the lowest N_{FB}.

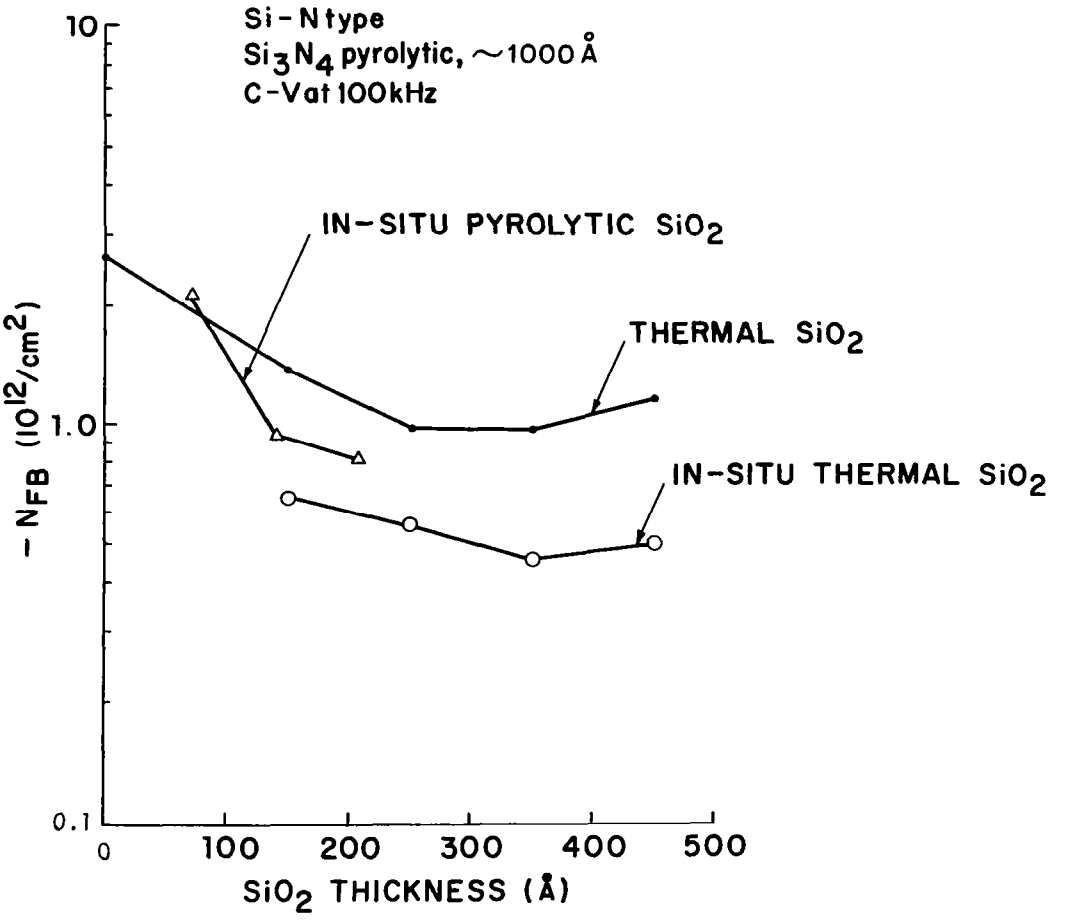


Fig. 31. N_{FB} vs. oxide thickness for MNOS wafers with three methods of oxide formation.

2.3.2 Stability

Stability of nitride and nitride-oxide films was investigated under applied field both at room-temperature and at elevated temperatures. Silicon nitride is very resistant to alkali ion motion,[16,17] but is subject to instabilities related to electron motion and trapping. In general, silicon nitride applied to bare silicon exhibits a "slow-state" type of instability.[18] This type of instability gives a ΔV_{FB} with the same sign as the stress bias. At room-temperature this instability can cause a hysteresis in the C-V trace. It was found that a threshold field must be exceeded before this room-temperature drifting occurs. For a wide range of deposition conditions (those in Table 1) this threshold was in the range of $1 - 2 \times 10^6$ V/cm. By depositing the nitride over a thin SiO_2 film, this threshold is raised to about 4×10^6 V/cm.

The room-temperature drift behavior of a number of wafers is shown in Fig. 32. By increasing the C-V bias sweep limit in steps and noting V_{FB} after each sweep, a plot of V_{FB} vs. peak field was obtained. The MNOS wafers were prepared by deposition in four different carrier gases and show typical thresholds of $\sim\pm 4 \times 10^6$ V/cm. Note that both polarization type (ΔV_{FB} having opposite sign as stress bias) and slow-state type of shifts are observed, but that slow-state shifts predominate at high fields. The MNS structure (4227, He carrier, 900°C, SiH_4:NH_3 = 1:10) shows only the slow-state shift and has a threshold of about $\pm 1.4 \times 10^6$ V/cm.

Bias-temperature stability measurements were performed on a variety of structures under different bias, temperature, and contamination conditions. The motion of sodium in pyrolytic silicon nitride was investigated by evaporating $Na^{22}Cl$ (10^{13} Na^+/cm^2) onto a 5700 Å nitride film (H_2 carrier, 850°C, SiH_4:NH_3 = 1:40). After evaporation of aluminum electrodes, 4 dots were given a sequence of +30V, 30 minute treatments at 200°C, 300°C, 400°C, and 500°C. V_{FB} and N_{FB} as a function of time for these and floating dots are shown in Fig. 33. Note that the shifts with 400°C and 500°C are in the opposite direction to that expected with sodium migration. After the 500°C treatment, the aluminum was etched off and an autoradiogram made. The absence of any images in the autoradiogram showed that the sodium never left the aluminum-nitride interface. For comparison, N_{FB} is plotted for a phosphosilicate stabilized SiO_2[19] sample (uncontaminated) under the same stress conditions. Ionic polarization at 400°C and 500°C are quite evident.

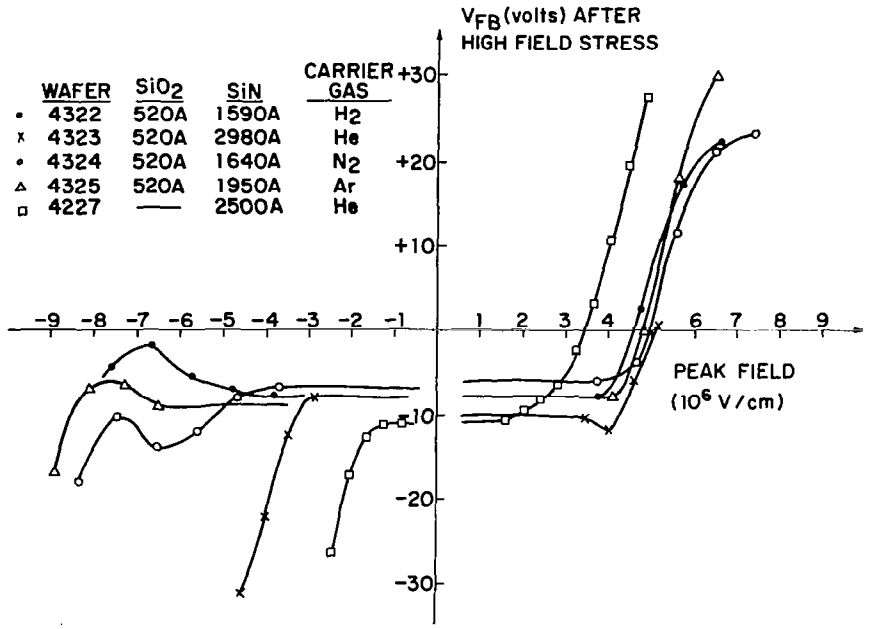


Fig. 32. Room-temperature drift in MNS and MNOS devices. V_{FB} is measured after sweeping C-V bias to a peak field. (Field = Bias/total thickness.)

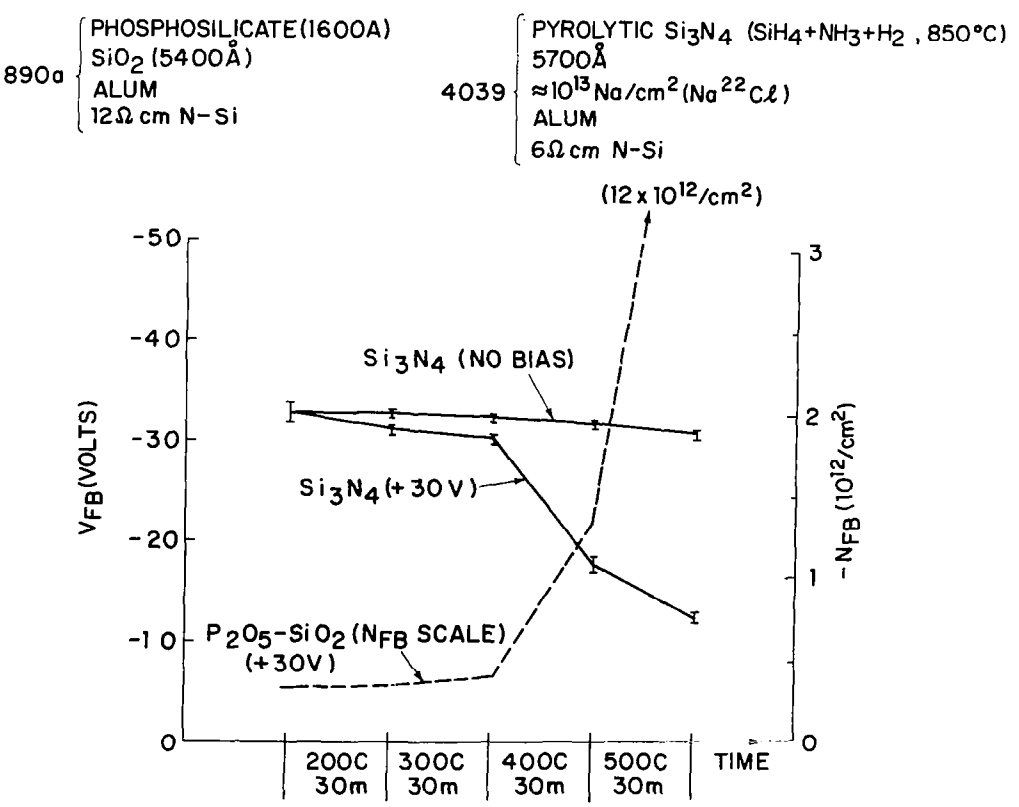


Fig. 33. V_{FB} and N_{FB} with bias-temperature stress sequence on Na^{22} contaminated pyrolytic silicon nitride and uncontaminated phosphosilicate-SiO_2 samples. The phosphosilicate data refer only to the N_{FB} scale.

It was found that the direction of shift ΔV_{FB}, for a given stress bias at elevated temperature, depends on the presence of an oxide layer under the nitride. The proposed mechanism for instability in the metal-nitride-silicon and metal-nitride-oxide-silicon structures is illustrated in Fig. 34. With positive bias applied to the MNS structure, electrons injected from the silicon into the nitride are trapped and cause a positive C-V shift. In the MNOS structure the oxide blocks injection of electrons from the silicon (unless fields are extremely high). Electronic con-

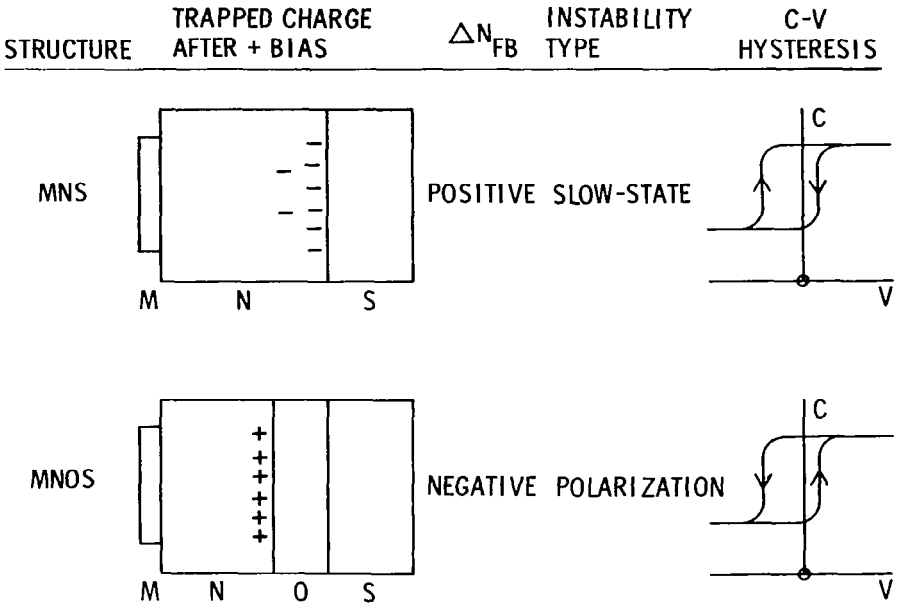


Fig. 34. Instability mechanisms in MNS and MNOS structures.

duction can still occur in the nitride, however, and this causes a positive space-charge layer to develop near the nitride-oxide interface giving a negative C-V shift. The resulting polarization type of instability can be avoided only by forming a silicon nitride film of extremely high resistivity. Resistivity of silicon nitride will be discussed in a later section. The stability differences between MNS and MNOS structures are clearly shown in Fig. 35. Here, devices were stressed at 200°C for 30 minutes at various fields. Sample 4361 had about 150 Å of in-situ thermal oxide (O_2, 1000°C). Both wafers had about 1000 Å of nitride (860°C, N_2 carrier, SiH_4:NH_3 = 1:20). In this figure the electric displacement D is specified rather than the average field E for bias-temperature stress. This is more meaningful than average field since D is continuous at the nitride-oxide interface (assuming no conduction), with electric field in each insulator being given

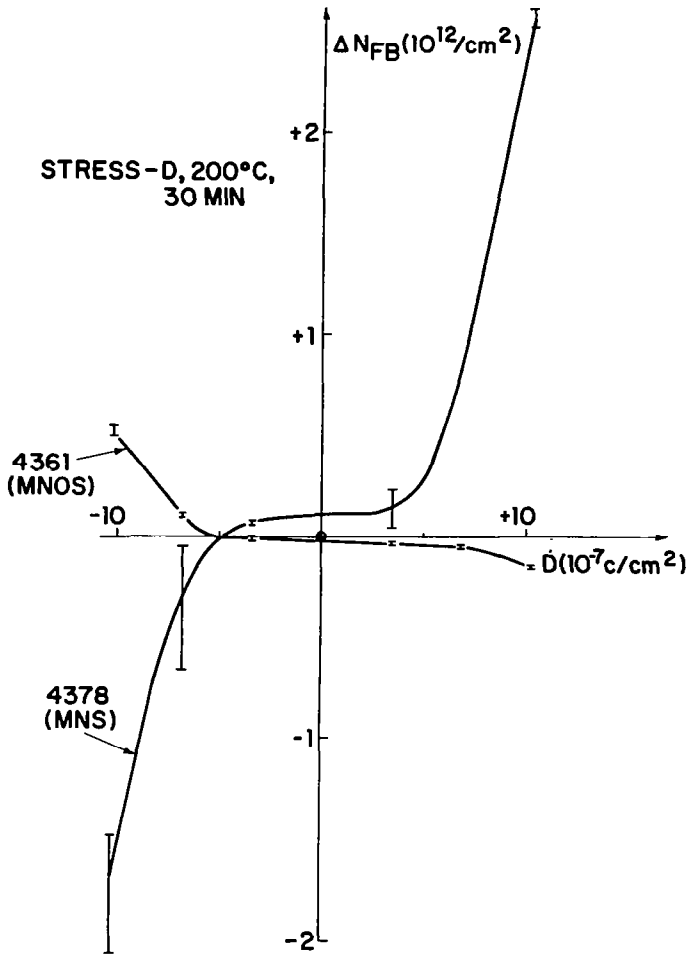


Fig. 35. Bias-temperature shift ΔN_{FB} for MNS and MNOS devices vs. electric displacement D applied for 30 minutes at 200°C.

by $E = D/\epsilon$. Taking the relative dielectric constants of SiO_2 and Si_3N_4 as 3.84 and 7.6, respectively, $D = 3.4 \times 10^{-7}$ coul/cm^2 corresponds to a field of 1×10^6V/cm in the SiO_2 and 0.505×10^6V/cm in the silicon nitride. Figure 35 shows that ΔN_{FB} is a non-linear function of D, with both structures having a threshold, below which shifts are small. As expected from the above model, the MNS shifts are in the slow-state direction, whereas the MNOS shifts are the polarization type. The MNOS structure is clearly more stable than the MNS structure at all bias levels.

Bias-temperature stability was measured for longer stress periods on a number of MNOS samples. Figure 36 gives V_{FB} vs. time under 200°C, $D = \pm 3.4 \times 10^{-7}$C/cm stress for three methods of oxide formation. The oxide and nitride deposition

processes were previously given in the discussion of Fig. 31. The film thicknesses and stress-bias levels are given for each wafer in Fig. 36. The wafer with in-situ thermal oxide appears to be the most stable — shifting less than 0.2 volts after 135 hrs. Samples with in-situ oxides up to 450 Å thick (see Fig. 31) were also tested and gave essentially the same stability as wafer 4361. The in-situ pyrolytic oxide (wafer 4387) wafer had a slow-state shift in the first 0.5 hr suggesting an $Si-SiO_2$ interface inferior to a thermal SiO_2-Si interface.

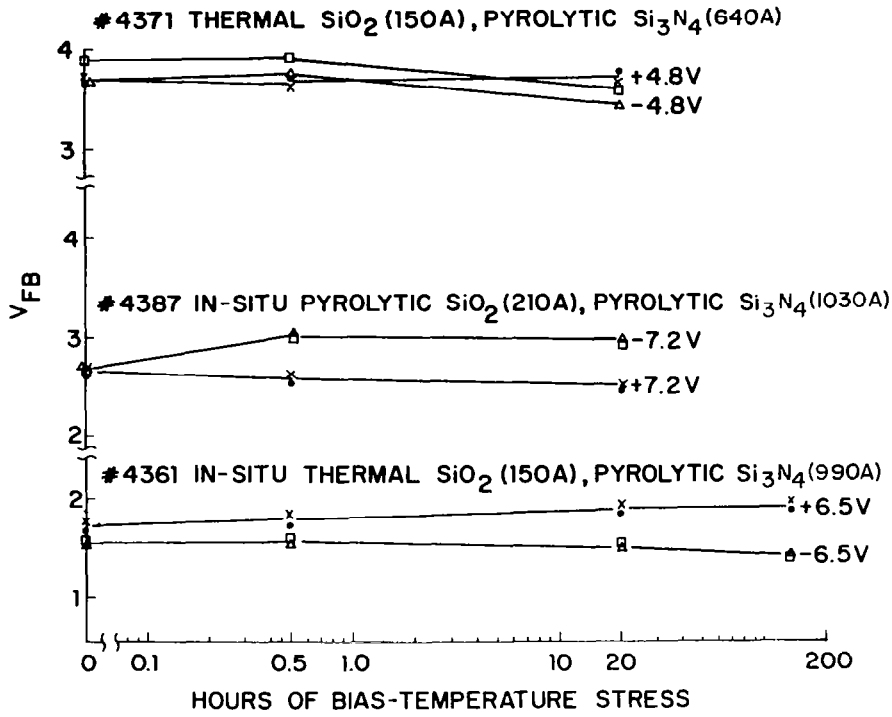


Fig. 36. V_{FB} vs. time under bias-temperature stress (200°C, $D = \pm 3.4 \times 10^{-7}$ C/cm) for MNOS samples with three methods of oxide formation.

2.3.3 Dielectric Constant

The dielectric constants of many films of pyrolytic silicon nitride have been determined by making accurate thickness measurements and capacitance/cm^2 measurement (in accumulated region of C-V curve). Since refractive indices were not known accurately, thickness measurements were made by the Tolansky[3] technique after etching in step in the film. Sharp steps were obtained by etching in concentrated HF with a chromium and wax mask. It was found that the measured

dielectric constants were independent of film thickness and showed no frequency dependence over the range 100 Hz to 1 MHz. Uncertainties in film thickness, electrode area, and capacitance indicated an absolute error of generally less than 3% in ϵ_r. Figure 37 shows ϵ_r vs. SiH_4:NH_3 ratio for films deposited in H_2 carrier gas. Note that ϵ_r has very little dependence on either the deposition temperature or the SiH_4:NH_3 ratio. A value of $\epsilon_r = 7.6$ appears to be the best average value for high ammonia fractions. Table 4 gives ϵ_r measurements for films deposited in other carrier gases. The conclusion is that the dielectric constant is not sensitive to the carrier gas used. As a check on the measurement method the dielectric constant of thermal SiO_2 was determined and agrees with the standard value.

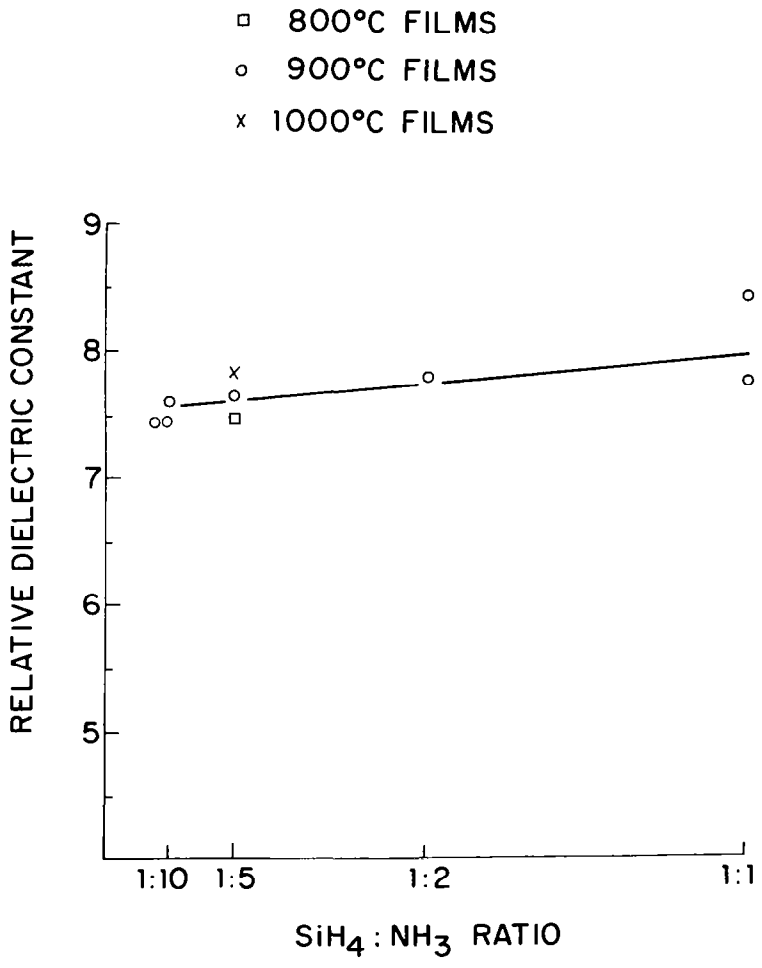


Fig. 37. Dielectric constant vs. silane:ammonia ratio for pyrolytic silicon nitride films deposited in H_2 carrier. Each data point represents an individual wafer. Measurements were at 25°C and 10 KHz.

TABLE 4. Relative Dielectric Constants of Pyrolytic Silicon Nitride Films.

Wafer	Depos. Temp. (°C)	Carrier	SiH_4:NH_3	ϵ_r
4195	900	He	1:10	7.4
4243	900	He	1:10	7.3
4260	900	He	1:10	7.4
4311	800	N_2	1:10	7.7
4295	900	N_2	1:20	7.5
4346	800	Ar	1:10	7.6
4347	900	Ar	1:10	7.6
4348	1000	Ar	1:10	7.6
4149 (SiO_2)				3.86

2.3.4 Electronic Conduction

At high fields ($E > 10^6$ V/cm) electronic leakage currents are observed in MNS structures at room temperature. These currents are characterized as being very reproducible between devices on a given wafer, being symmetrical with respect to polarity of dc bias, showing no decay with time, and having a very non-ohmic I-V characteristic. In fields normally experienced by passivation layers, these currents are negligible compared to junction leakage levels. However, as shown in the previous section on stability, electronic leakage in silicon nitride can cause space-charge build-up in the film and instability of N_{FB}. It is thus important that electronic leakage be minimized. A typical measurement on a rather thick film of pyrolytic silicon nitride is shown in the log I vs. log V plot of Fig. 38. Note that current changes by seven orders of magnitude for less than a factor-of-three change in bias. The log I vs. log V behavior appears to be roughly linear down to extremely low currents. Because of the limited range of V, however, good linearity is also obtained if one plots log I vs. $V^{1.2}$. I-V measurements were made on a number of wafers with variations in nitride deposition. With identical deposition conditions, films of varied thickness gave coincident curves if log I vs. $E^{1/2}$ was plotted. The currents are thus field controlled rather than voltage controlled. Log I vs. $E^{1/2}$ plots generally had the same slope, but were shifted along the $E^{1/2}$ axis by variations in the deposition process. This is illustrated in Fig. 39 for films deposited in H_2 carrier gas at 900°C with various SiH_4:NH_3 ratios. Note

that changing the ratio from 1:1 to 1:10 causes the field required for any given current level to increase by about a factor of five. Increasing the ammonia fraction beyond the 1:10 ratio causes very little additional shifting of the characteristic. The theoretical slopes shown in Fig. 39 will be discussed later. Additional measurements showed that the leakage is not strongly influenced by deposition temperature.

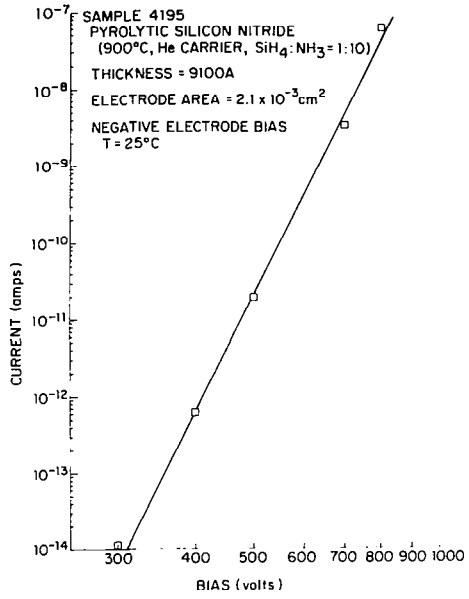


Fig. 38. Typical I-V data for a pyrolytic silicon nitride film.

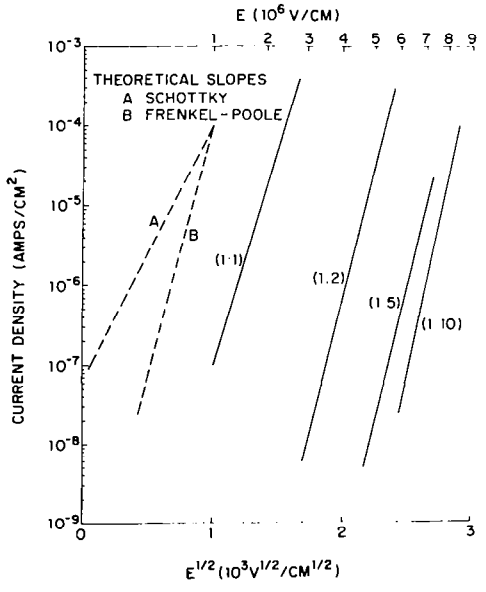


Fig. 39. Electronic leakage in pyrolytic silicon nitride films deposited at 900°C with H_2 carrier gas. Measurements are at 25°C, and the silane:ammonia ratios are given in parenthesis on each curve.

Four films deposited at 900°C with He carrier gas and varied SiH_4:NH_3 ratios were measured. Although the log I vs. $E^{1/2}$ slopes were similar to those observed with H_2 carrier gas, the effect of varying SiH_4:NH_3 was surprisingly small. Table 5 gives the field for current densities of 10^{-6} amp/cm^2 as a function of SiH_4:NH_3. Note that the dependence on SiH_4:NH_3 is much weaker than shown in Fig. 39 and, in fact, goes in the opposite direction.

TABLE 5. Effect of SiH_4:NH_3 on Electronic Conduction of Nitride Films Deposited at 900°C in He Carrier.

Wafer	SiH_4:NH_3	Field for $I/A = 10^{-6}$ A/cm^2 (10^6V/cm)
4284	1:1	±5.6
4285	1:5	±5.3
4286	1:10	±5.0
4287	1:20	±4.7

A linear relation between log I and $E^{1/2}$ suggests a Schottky barrier injection from the electrodes as the conduction mechanism. However, the symmetry with bias polarity and the slope of log I vs. $E^{1/2}$ curves indicate that this is not the mechanism. The Schottky equation for emission into an insulating film is

$$I/A = \Lambda T^2 \exp \frac{q}{kT} \left[\left(\frac{qE}{4\pi\epsilon} \right)^{1/2} - \varphi \right]$$

where Λ is the Richardson constant, φ is the interfacial barrier height, and ϵ is the optical dielectric constant of the insulator. The slope of this function (log I/A vs. $E^{1/2}$) is shown in Fig. 39 for T = 300°K and $\epsilon = 4\epsilon_o$. This optical dielectric constant of 4 is obtained by squaring the refractive index. Note that the experimental curves have a considerably higher slope than predicted by the Schottky equation. A more probable conduction mechanism is the emission of carriers from traps in the bulk of the film (Frenkel-Poole[20] model). This model leads to the equation

$$I/A = \sigma_o E \exp \frac{q}{kT} \left[\frac{1}{r} \left(\frac{qE}{\pi\epsilon} \right)^{1/2} - \frac{\varphi}{r} \right]$$

where σ_o is a constant, φ is the trap energy level measured from the conduction band, ϵ is the optical dielectric constant, and r is a variable ranging from 1 to 2 depending on the Fermi level in the insulator being below or above the trap level, respectively. Although E appears in front of the exponential in this equation, its limited range of variation permits an approximately linear dependence of log I/A on $E^{1/2}$. Note that with $r = 2$ the slope of log I/A vs. $E^{1/2}$ will be the same as given by the Schottky equation. With $r = 1$ the slope will be twice the Schottky slope. The theoretical Frenkel-Poole slope for $r = 1$, $T = 300^{o}K$, $\epsilon = 4\epsilon_o$ is shown in Fig. 39 and is a fairly good fit to the experimental curves.

2.3.5 Electrical Measurements on Silicon Oxynitride

As mentioned in other sections of this report, oxygen may be added to the pyrolytic reaction to produce silicon oxide-silicon nitride mixtures having higher etch rates than pure nitride but still acting as a barrier to high temperature steam. A limited number of electrical measurements have been made on such films and are summarized in Table 6. The effect of film deposition temperature and the effect of an underlying thermal oxide were examined. N_2 carrier gas was used in all cases, and the SiH_4:NH_3:O_2 ratios are given in Table 6. By comparing these data with earlier data for pure silicon nitride, the following conclusions were reached: The dielectric constants for the mixtures are between those of SiO_2 and Si_3N_4, as expected. Room-temperature drift thresholds are well above those of pure nitride ($1\text{-}2 \times 10^{6}$ V/cm), except for one anomalous wafer. When applied to bare silicon, N_{FB} levels for the mixtures are not significantly lower than found with pure nitride. As found with pure nitride, a thin (150 Å) underlying thermal oxide significantly reduces N_{FB} and improves bias-temperature stability. The ΔN_{FB} shifts are comparable to those observed with pure nitride.

TABLE 6. Electrical Measurements on Nitride-Oxide Mixtures

Wafer No.	4389	4390	4393	4394	4395	4396
Thermal oxide	none	150A	none	none	none	none
Nitride-Oxide Deposition Temp(°C)	850	850	700	800	900	1000
$SiH_4:NH_3:O_2$	1:10:1	1:20:1	1:20:0.5			
Dielectric constant	-	-	4.8	5.5	5.2	6.1
Rm-temp. drift threshold (10^6V/cm)	6-7	5	3.1	1.6	4.5	4.0
$-N_{FB}$ before anneal ($10^{11}/cm^2$)	24	6.5	16	19	13	18
$-N_{FB}$ after 300°C, N_2, 30m ($10^{11}/cm^2$)	18	5.7				
ΔN_{FB}, + bias,* 200°C, 30 m ($10^{11}/cm^2$)	-0.3	-0.2				
ΔN_{FB}, + bias,* 200°C, 20 h ($10^{11}/cm^2$)		-0.6				
ΔN_{FB}, - bias,* 200°C, 30 m ($10^{11}/cm^2$)	-1.8	-0.6				
ΔN_{FB}, - bias,* 200°C, 20 h ($10^{11}/cm^2$)		-1.1				

*Bias gives $D = \pm 3.4 \times 10^{-7}$ Coul/cm^2.

3.0 DIFFUSION MASKING EFFECT

The diffusion masking effect of the pyrolytic silicon nitride for common dopants in silicon has been investigated previously and has been reported in literature.[21] Later, this study was extended to the aluminum diffusion into silicon and zinc diffusion into gallium arsenide. It is well known that silicon dioxide fails to mask oxygen, gallium, aluminum and zinc diffusion at elevated temperature. On the other hand, the pyrolytic silicon nitride masks all those elements. Figures 40-42 show the beveled and junction delineated silicon which have been partly masked with silicon nitride and diffused by oxygen, gallium and aluminum respectively. Figure 43 shows the beveled and junction delineated gallium arsenide which has been partly masked by silicon nitride and diffused with zinc. Note in all diffusions, the silicon nitride effectively resisted diffusant penetration. The silicon nitride thickness, the diffusion temperature and time, the surface concentration (C_o) of diffusant and the junction depth (x_j) measured in the unmasked regions were shown in Table 7. In many cases, a very thin film of silicon nitride masks dopant diffusion.

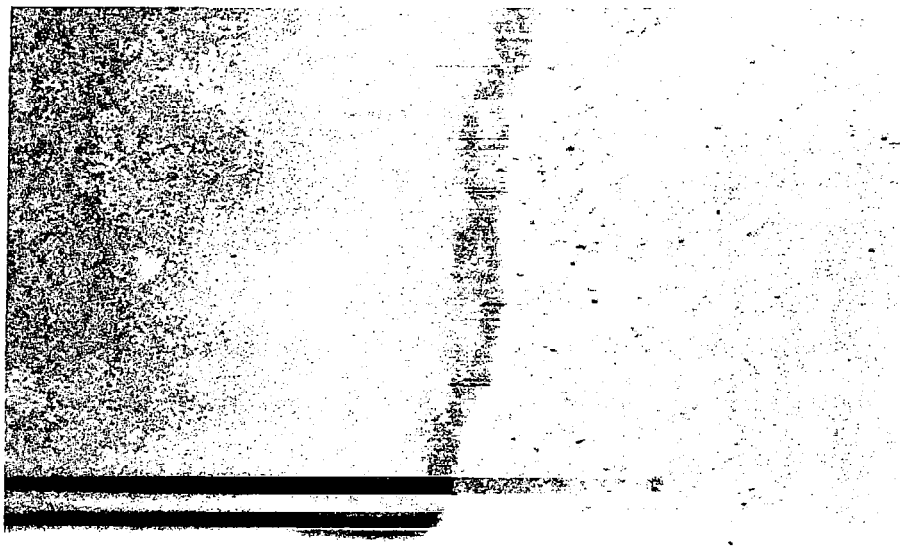


Fig. 40. Silicon nitride mask for steam oxidation.

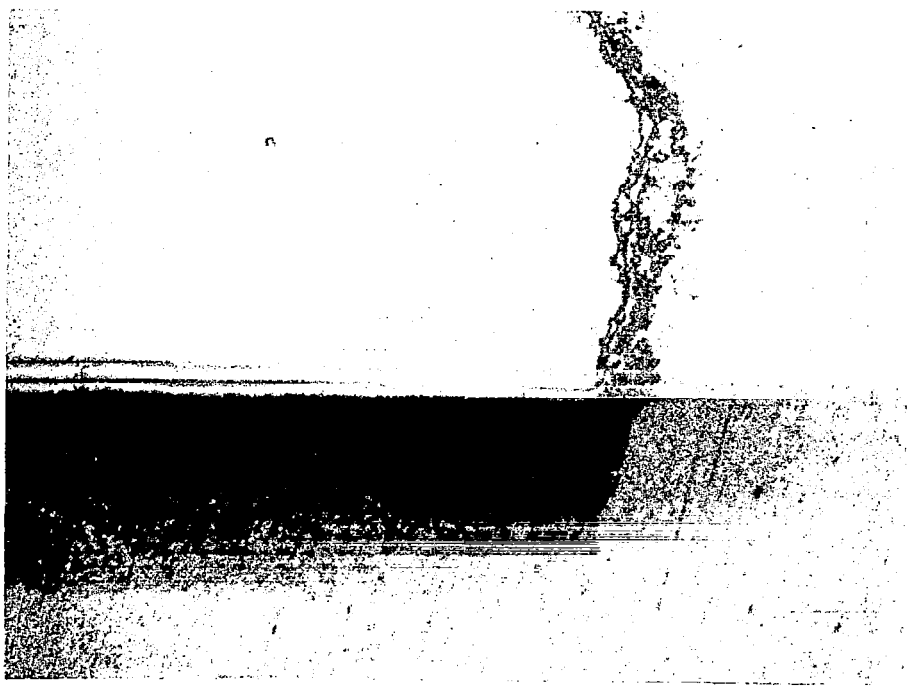


Fig. 41. Silicon nitride mask for Ga diffusion.

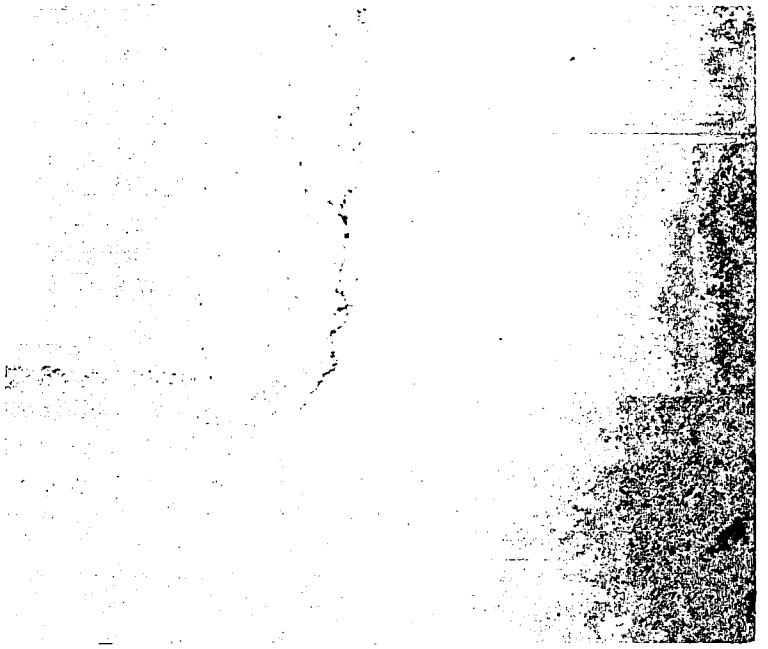


Fig. 42. Silicon nitride mask for Al diffusion.

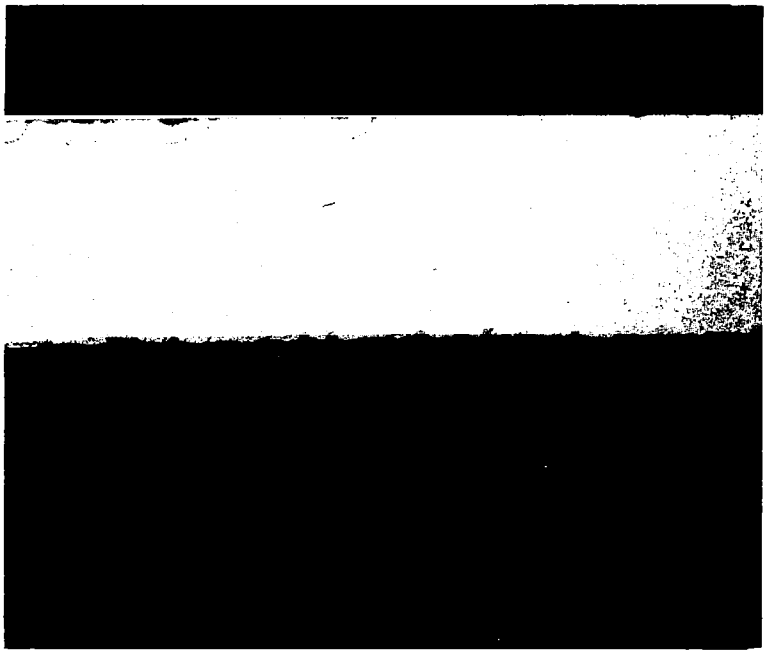


Fig. 43. Silicon nitride mask for Zn diffusion.

TABLE 7. Silicon Nitride as a Diffusion Mask for Various Dopant Elements.

Diffusant	Temp (°C)/Time (min)	$C_o(cm^{-3})$	x_j (μ)	Mask Thick. (Å)
B	1108/60	5×10^{20}	2.78	~350
P	1050/67	1×10^{21}	1.77	~350
As	1108/149	1.8×10^{21}	1.9	~350
Ga	1108/146	2.1×10^{19}	2.78	~350

Further investigation was made to determine the minimum film thickness required to mask the diffusion of the most common dopants (B, P, As and Ga) for silicon. About 1000 Å of silicon nitride was deposited on 0.1 ohm-cm both N- and P-type silicon wafers. The nitride films were etched to various thickness steps, 200, 350, 500, 700 and 1000 Å. The diffusion conditions and the resulting surface concentrations and junction depth in unmasked regions are shown in Table 8. The results confirmed previous report,[15] i.e., only a very thin layer of silicon nitride is required to mask the diffusion of all the dopants.

TABLE 8. Minimum Silicon Nitride Thickness for Masking Common Dopant Diffusion for Silicon.

Substrate	Si_3N_4 Thickness (Å)	Diffusion Temp (°C)/Time (min)			X_j (μ)	C_o (atoms/cc)
		Diffusant	Deposit	Drive-in	w/out mask	w/out mask
Si	900	Al		1108/120	6.5	1.4×10^{19}
Si	1200	B	980/30	1200/30	2.07	7×10^{19}
Si	1200	P	1100/10	1100/20	1.8	1×10^{21}
Si	150	As		1200/120	1.44	1.4×10^{20}
Si	250	Ga		1100/90	3.2	4×10^{19}
Si	250	O		1150/20	0.5	—
Ge	250	Ga		800/120	0.92	1×10^{19}
GaAs	600	Zn	750/16 hrs	850/120	8.0	—

3.1 PHOTO-ETCH TECHNIQUES

In applying silicon nitride to integrated circuits on devices for masking dopant diffusion and/or for surface passivation, the pyrolytically deposited silicon nitride films must be photo-etched without great difficulties. Earlier attempts[15] using the reverse sputtering technique showed encouraging results. Windows of about 0.1 - 0.2 mil dimensions have been successfully opened with the help of ordinary photoresist as mask. The apparatus used for hot H_3PO_4 etch of silicon nitride is shown in Fig. 44.

Fig. 44. Apparatus for hot H_3PO_4 etch of silicon nitride.

Because the etch rate of pyrolytic silicon nitride in 48% HF is very low (~ 100 Å min^{-1}), conventional photoresists are unable to stand prolonged etch. Since many metals are not attacked by 48% HF, yet can be photoengraved with convention photoresists, metal masks were tried for photoengraving silicon nitride films. Both chromium and molybdenum films have been successfully used as a mask for silicon nitride etch. The metal film about 1000-1500 Å can be deposited onto the nitride by evaporation, sputtering or pyrolytic chemical deposition. By using conventional photolithographic methods, windows are opened in the metal film. Chemicals for etching metal masks are potassium ferrocyanide solution for chromium, and nitric acid solution for molybdenum. Then the windows in silicon nitride are etched out with 48% HF. Finally, the metal film is removed. Figure 45 shows windows that have been opened in silicon nitride with a chromium mask (~ 1200 Å Cr). The definition in both 500 Å (Fig. 45A) and 1330 Å (Fig. 45B) nitride films is sharp.

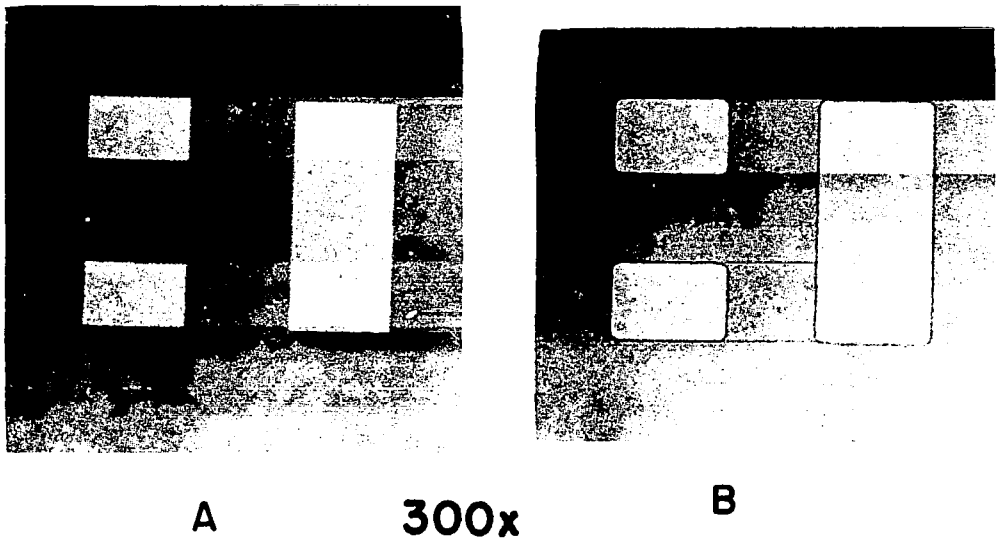


Fig. 45. Windows in silicon nitride opened with Cr mask. Film thickness = A. 500 Å, B. 1330 Å.

There are some shortcomings with metal masks. Poor adhesion of metal films on nitride is often observed when the nitride has not been cleaned adequately prior to metal deposition. Also pinholes were sometimes found in the metal films. Any residual metal on the nitride surface resulting from inadequate removal and cleaning may have an adverse effect in subsequent processing.

Recently, a phosphoric acid (H_3PO_4) etch of silicon nitride was proposed by VanGelder and Houser.[2] At 180°C, the acid (~91% vol.) etches pyrolytic silicon nitride at about the same rate as 48% HF at room temperature (~ 100 Å min^{-1}). However, it does not etch silicon dioxide appreciably. Therefore, silicon dioxide can be used as mask for nitride etch. In reality, many difficulties have been experienced. Generally silicon nitride is deposited on an oxidized silicon substrate followed by a deposition of pyrolytic oxide as mask; thus, a three layer ONO (oxide-nitride-oxide) film is formed. In photoetching pyrolytic oxide in the windows with buffered HF, it is found that the etch time required is much longer than that for etching a blank wafer which has no photoresist. Because of the refractive index difference of the ONO-layers, it is extremely difficult to determine when the pyrolytic oxide is etched off completely. Before further etching of the silicon nitride in the windows in hot H_3PO_4, the photoresist must be removed. It is often found that the time required to etch through the silicon nitride is also much longer than expected. This is apparently due to the presence of a thin residue of pyrolytic oxide in the windows. It is also difficult to judge whether the silicon nitride has been etched through.

Most difficulties could be due to the presence of photoresist residue in the windows, etch rate variation with window size, and the peculiar etching behavior of pyrolytic oxide deposited on nitride and the nitride deposited on thermal oxide which has gone through dopant diffusions. These problems are yet to be answered.

In spite of the difficulties in photoetch, many samples have been successfully photoetched in hot H_3PO_4. The etched pattern is shown in Fig. 46. Note the sharp definition. Thus basically, the technique is sound and very attractive for integrated circuit applications.

3.2 SILICON NITRIDE PASSIVATED DIODES AND INTEGRATED CIRCUITS

Although the electrical properties of the silicon nitride-silicon interface have been investigated by the capacitance measurement on the MNS samples, the passivation property of silicon nitride on silicon should be ultimately tested on devices and integrated circuits. For this purpose diodes and integrated circuits were fabricated.

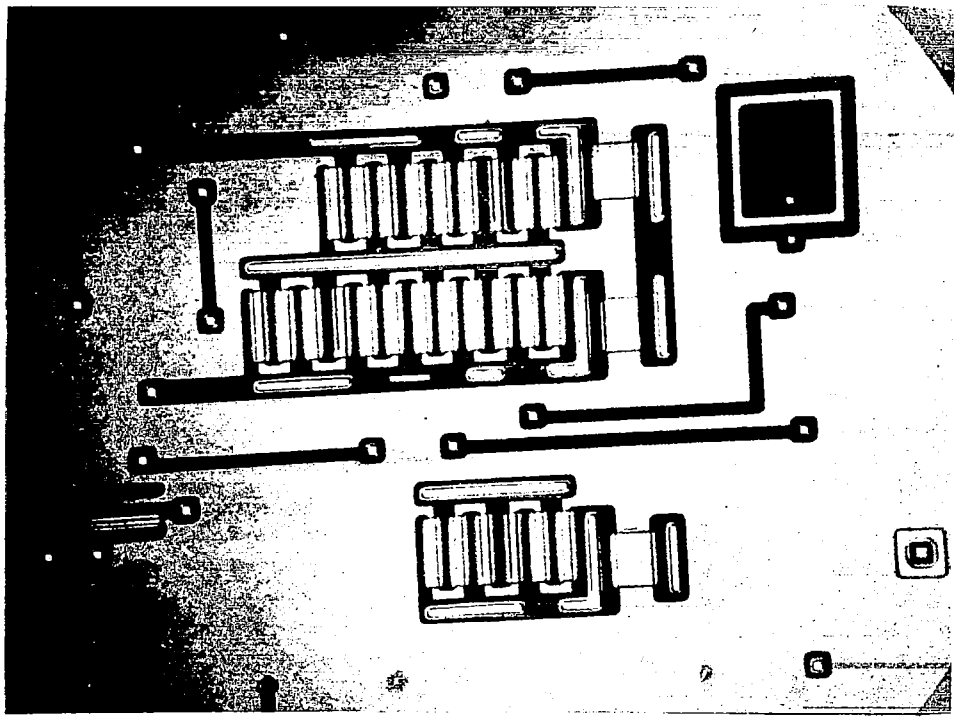


Fig. 46. Photoetched silicon nitride-silicon dioxide two layer film by using hot H_3PO_4 with pyrolytic oxide as a mask. Magnification 170X

3.2.1 Silicon Nitride and Oxide Passivated Diodes

Composite layers of silicon nitride and silicon dioxide have been used as junction diffusion masks and as a surface passivation dielectric. The substrates were N-type silicon of about 1 Ω-cm. Thin layers of silicon dioxide ranging from 150-450 Å were grown by oxidation in dry oxygen. This was followed by the deposition of a layer (~ 1000 Å) of silicon nitride. Over the silicon nitride, a 2000 Å pyrolytic oxide was deposited to provide an etching mask for the silicon nitride. Windows were opened through the pyrolytic oxide by the conventional photoetch method. After the photoresist was removed, the wafers were etched in hot H_3PO_4 to open windows in the silicon nitride film. Finally the windows were etched all the way down the substrate silicon with a buffered HF solution. The boron diffusion consisted of deposition at 1050°C for 50 minutes and drive-in at 1100°C for 35 minutes. The reverse bias breakdown voltage and the leakage current of the diodes were measured on a curve tracer. A 60 volt breakdown voltage with leakage currents less than 1μA was obtained. Figure 47 shows the typical I-V curve of the Si_3N_4-SiO_2 passivated diodes.

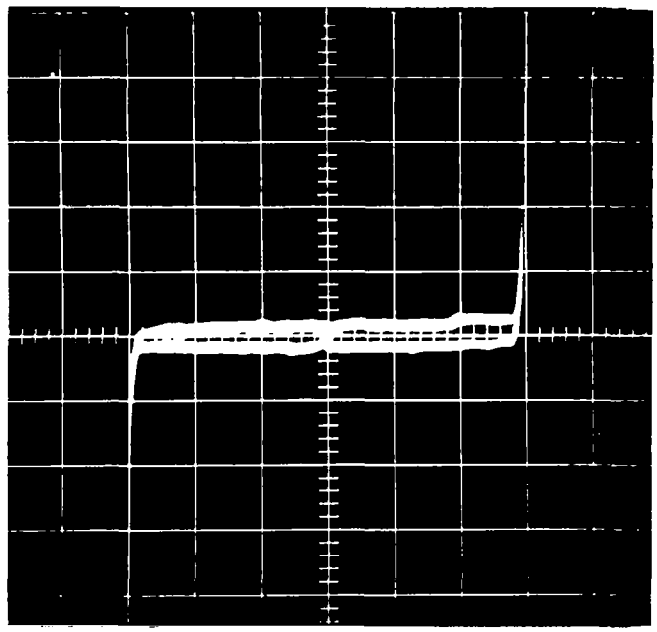


Fig. 47. Reverse bias breakdown of back to back diodes passivated with SiO_2 (200 Å) + Si_3N_4 (950 Å) which was also used for masking B diffusion, 1050°C / 60 min deposition plus 1105°C / 35 min drive in. Scales = Horizontal 1 division = 20 volts; vertical 1 division = 0.01 ma.

3.3.2 Silicon Nitride and Oxide Passivated Integrated Circuits

Since the main objective of this work is to test the passivation properties of silicon nitride and oxide against the contaminants such as sodium and moisture which often cause serious degradation in the electrical parameters of the devices in silicon integrated circuits, the detailed nature of the integrated circuit itself is of secondary interest. Several IBM standard integrated circuit wafers have been processed. The integrated circuit used in this investigation was designed, developed and funded by IBM.

The integrated circuits have three resistors and one large and two small transistors. The large transistor consists of 12 transistors which are connected in parallel to form a common base, collector and emitter configuration. The terminals of the resistors and the transistors are brought out to separate pads so that the electrical properties of the individual components may be characterized. The circuit diagram and the top view of the IC chip are shown in Figs. 48 and 49 respectively.

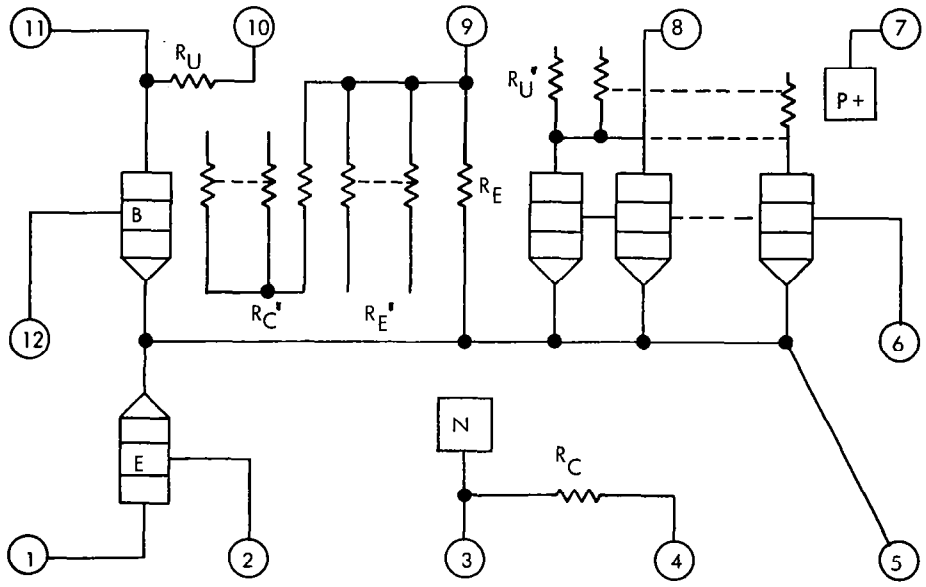


Fig. 48. Circuit diagram.

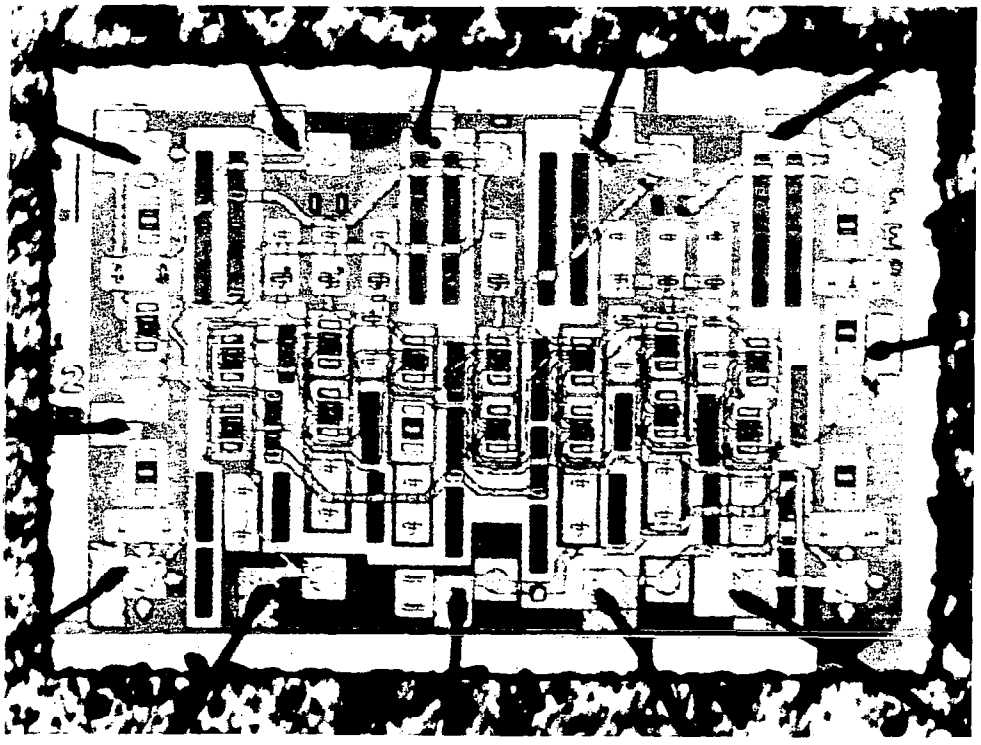


Fig. 49. Top view of the circuit chip. Magnification 120X

The IC wafers are fabricated by the planar multiple diffusion technology. A layer of n-type epitaxy is grown over the P^- type silicon substrates. The individual components to be fabricated are isolated electrically by a P-type (boron) diffusion. A second boron diffusion is then performed to form the resistors and the base of the transistors. The n-type (phosphorous) diffusion is subsequently performed to form the emitters of the transistors. It is followed by the deposition of a 1000 Å film of silicon nitride and then a layer of pyrolytic oxide ~3000 Å over the entire wafer. Contact holes were then opened by using the photoetch processes described in Section 3.2. The wafers were then aluminized, alloyed, and photoetched to provide interconnections. Finally, the wafers were diced and mounted on 12-pin TO-5 headers. Gold wires of 0.5 mil diameter were attached to the aluminum pads (on chips) and the pins.

During testing, it was found that most circuits and transistors were open due to the broken gold wires at the aluminum pads. Additional gold wires were then attached. To prevent the breaking of the gold wire contact during handling, a metal cap was loosely placed on each header. About 300 Å of sodium chloride was evaporated onto a number of mounted chips before the caps were placed on the headers.

The transistors were tested at 175°C. The cut-off conditions were collector to base bias, V_{CB} = 8 volts and emitter to base bias, V_{EB} = 4 volts with isolation at base potential. Periodic readouts of the following parameters were made using the Fairchild 4000 M/1620 Tester:

H_{FE} @ V_{CB} = 0.0, I_E = 0.001, 0.01, 0.1 ma
BV_{CBO} @ 10μa and I_{CBO} @ several voltages <BV
BV_{EBO} @ 10μa and I_{EBO} @ several voltages <BV
BV_{CEO} @ 1 ma and I_{CEO} @ several voltages <BV
BV_{ISO} @ 10μa and I_{ISO} @ several voltages <BV

where H_{FE} is the current gain; BV is the breakdown voltage; BV_{CBO}, BV_{EBO}, BV_{CEO} and BV_{ISO} are the breakdown voltages at the collector to base, emitter to base, collector to emitter, and the isolation junction, respectively; and I_E, I_{CBO}, I_{EBO}, I_{CEO} and I_{ISO} are the measured currents of emitter, collector to base, emitter to base, emitter to collector and isolation junction, respectively.

Initial measurements showed substantial chip to chip variation in H_{FE}, V_{CBO} and V_{ISO}. (The heating steps for the deposition of silicon nitride and pyrolytic oxide, as nitride etch mask are at least partly responsible for the chip to chip variations in initial measurements.) The devices are not designed to take additional heating steps for nitride and oxide depositions. Those additional steps caused junction movement as evidenced in low BV_{ISO} and high H_{FE}.

The results on thermal and electrical stress tests are listed in Tables 9-12.

TABLE 9. The H_{FE} Changes in Silicon Nitride Passivated Circuit Transistors.

H_{FE} @ $I_E = 100\mu a$, $V_{CB} = 0$

Tx	t=0	t=96	t=190	t=285	t=375	t=666	ΔH_{FE}	t_{max}
1-1	58.0	-	21.9	22.4	22.7	34.62	-36.1	190
1-2	35.2	38.1	38.6	35.5	35.3	34.54	+3.4	190
1-3	49.9	18.4	18.9	19.2	19.2	17.52	-32.38	666
3-1	31.3	32.1	31.6	31.9	31.7	58.8	+27.5	666
3-2	40.2	37.6	35.6	35.0	34.4	33.2	- 7.0	666
3-3	106.5	96.4	35.6	30.6	29.7	23.1	-83.4	666
4-1	32.2	31.6	30.9	30.6	30.1	29.1	- 3.1	666
4-2	31.6	32.5	32.7	33.1	33.2	27.5	- 4.1	666
4-3	25.9	26.4	26.3	26.2	26.2	15.1	-10.8	666
5-1	31.2	29.7	-	30.4	30.3	-	- 1.5	96
5-2	33.6	34.2	34.5	35.0	34.5	28.8	- 4.8	666
5-3	43.1	45.5	44.4	43.9	43.0	-	+ 2.4	96
6-1	114.6	27.4	37.5	28.8	24.2	-	-90.4	375
6-2	21.0	16.8	16.1	15.9	16.7	26.8	+ 5.8	666
6-3	41.4	43.8	-	39.0	44.2	40.9	+ 2.8	375
7-1	34.1	29.4	29.1	28.5	38.4	31.2	- 5.6	285
7-2	32.1	14.7	14.5	15.4	22.9	26.6	-17.6	190
7-3	28.0	20.6	19.5	19.5	19.7	24.9	- 8.5	190&285
8-1	92.0	87.3	49.0	51.2	51.8	45.3	-46.7	666
8-2	66.2	62.4	46.8	43.5	27.3	30.8	-38.9	375
8-3	12.4	20.7	18.9	46.1	30.1	-	+33.7	285

TABLE 10. The BV_{CEO} Changes in Silicon Nitride Passivated Circuit Transistors.

	BV_{CEO} @ 1 ma					(no entry = no change)
Tx	t = 0	t = 96	t = 190	t = 285	t = 375	t = 666
1-1	3.3					
1-2	3.6					
1-3	3.1					
3-1	6.3					
3-2	6.2					
3-3	5.5		6.2			6.7
4-1	6.4					
4-2	6.4					
4-3	5.5					
5-1	4.8					
5-2	4.8					
5-3	4.2					
6-1	11.7		13.7	11.8		14.6
6-2	12.1					15.7
6-3	6.2					
7-1	6.4					
7-2	6.5					
7-3	7.3					
8-1	5.6		5.9		6.2	
8-2	6.0				6.4	
8-3	6.7				6.3	

TABLE 11. The BV_{EBO} Changes in Silicon Nitride Passivated Circuit Transistors.

no entry = <100 mV change

Tx	t = 0	t = 96	t = 190	t = 285	t = 375	t = 666
Tx 1-1	6.4					
1-2	6.4					
1-3	6.4					
Tx 3-1	6.4					
3-2	6.4					
3-3	6.2					
TX 4-1	6.4					
4-2	6.4					
4-3	6.4					
Tx 5-1	(isoshort.)	6.4				
5-2	to collec-	6.4				
5-3	tor	6.4				
Tx 6-1	18.1					
6-2	18.1					
6-3	6.4					
Tx 7-1	5.2	1.0	6.4			
7-2	5.2	1.0	6.4			
7-3	5.4	1.0	6.3			
Tx 8-1	6.4					
8-2	6.2					
8-3	6.4					

TABLE 12. The BV_{ISO} Changes in Silicon Nitride Passivated Circuit Transistors.

no entry = No change

Tx	t = 0	t = 96	t = 190	t = 285	t = 375	t = 666
1-1	24.1					
102	24.3					
1-3	24.2					
3-1	19.1					
3-2	19.0					
3-3	15.7					
4-1	26.4					
4-2	26.4					
4-3	26.3					
5-1	4.7					
5-2	4.9	Lower than BV_{CBO} so opened				
5-3	4.0					
6-1	25.8					
6-2	26.5					
6-3	26.4					
7-1	13.3	9.2	12.7	13.1		
7-2	13.5	8.0	11.9	13.0		14.2
7-3	4.9	1.2	4.5	4.8		
8-1	26.2					
8-2	26.3					
8-3	19.9					

All $I_{ISO} < 20\,nA$ @ $\frac{BV_{ISO}}{2}$

Chips 1, 3, 4 and 5 are not intentionally contaminated while the chips 6, 7 and 8 have received a deposition of about 300 Å of sodium chloride. As mentioned above, No. 1 and 2 are single transistors while No. 3 is the large transistor. Table 9 shows the changes in H_{FE} at $I_E = 100\mu a$ and $V_{CB} = 0$. The H_{FE} is measured at low emitter current level so that the surface recombination effect on H_{FE} becomes predominant. Note that in some tests no H_{FE} value was recorded, e.g., the transistor 1.1 at t = 96. This does not mean that the transistor went bad, but

rather that the computer relay has made poor contact and thus mis-printed the result. The testing hours are represented by t. Six readouts have been made at t = 0, 96, 190, 285, 375 and 666 hours. ΔH_{FE} is the maximum change in H_{FE} and t_{max} represents the hours that the units have been stressed when the readouts are made. Note that the initial large variation from 12.4 on the unit 8-3 to 114.6 on the unit 6-1. After being stressed for 666 hrs, the H_{FE} variation has been reduced down to 15.1 on the unit 4-3, and to 58.8 on the unit 3-1. Note that the large transistors, which consist of 12 transistors, showed that their H_{FE} has been more or less stabilized by the stressing. It is particularly interesting to note that the chips 6, 7 and 8 which have been contaminated by sodium chloride indicated little difference from the other chips. In fact, units 6-3 and 7-3 are among the best units. This clearly demonstrates that the silicon nitride has prevented sodium degradation of device characteristics. Large ΔH_{FE} is mainly due to its initial unusually high value. The stressing has helped to bring their value to that comparable to other units.

Tables 10, 11 and 12 show the changes in BV_{CEO}, BV_{EBO} and BV_{ISO} respectively. After 666 hrs stressing most transistors show no change. In some samples, the BV_{CEO} values have increased slightly. The increase corresponds to the decrease in H_{FE} values.

4.0 CONCLUSION

The method of preparing silicon nitride by the reaction of silane and ammonia has been extended to include nitrogen, helium and argon as carrier gases. Films grown in nitrogen and helium are superior to those grown in hydrogen or argon. The investigation was also extended to the growth of silicon oxynitride which has exhibited interesting masking properties for high temperature steam oxidation.

The properties of the silicon nitride which have been investigated include the refractive index, chemical etching, and electrical measurements. The electrical measurements on MNS (metal-nitride-silicon) and on MNOS (metal-nitride-oxide-silicon) samples revealed the information on flat band charge density, high temperature stability, dielectric constant and electronic leakage current. The MNOS samples exhibited reasonably low flat band charge density and excellent high-temperature and room-temperature stability.

Integrated circuits and diodes have been passivated with silicon nitride and the transistors have been tested under thermal and electrical stress. Little effect was found with intentional sodium chloride contamination as compared with non-contaminated integrated circuits after being stressed 666 hrs at 175°C cut-off (V_{CB} = 8 volts and V_{EB} = 4 volts).

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6.0 TECHNICAL CONFERENCES & PRESENTATIONS

1. April 13, 1966	The technical contract monitors, Dr. Phillip H. Klein and Mr. Robert L. Trent toured the IBM Components Division, East Fishkill facility. General discussions of contract requirements and technical approaches to meeting objectives were held. (Dr. V.Y. Doo, Dr. G.A. Silvey)
2. June 2, 1966	Dr. G.A. Silvey and Mr. A. Kran met with Dr. P.H. Klein at the NASA Electronics Research Center to review technical progress and content of the forthcoming report.
3. Aug. 9, 1966	Dr. P.H. Klein was given briefings at IBM East Fishkill by Drs. V.Y. Doo and G.A. Silvey on the status of vapor deposited silicon nitride development. Dr. D.R. Kerr described the associated electrical measurements.
4. Oct. 9-14, 1966	Drs. V.Y. Doo and D.R. Nichols presented the paper "Effect of Reactant Composition on Pyrolytic Silicon Nitride Films" at the Philadelphia Meeting of the Electrochemical Society - Abstract No. 146.
5. Nov. 22, 1966	Dr. V.Y. Doo gave an informal contract progress presentation at NASA-ERC, which was attended by personnel from the Materials, Failure Mechanisms and Microelectronics Branches.
6. Jan. 26, 1967	The formal contract presentation was held at NASA ERC. Dr. V.Y. Doo summarized the program status and gave a technical review on vapor deposited silicon nitride. Dr. D.R. Kerr discussed the related electrical measurements.

7. March 28, 1967 Mr. I. Lagnado and Mr. J. Bowe visited IBM E. Fishkill for a review of the silicon nitride work and a discussion of potential applications. Meetings were held with Dr. V.Y. Doo, Dr. G.A. Silvey, Dr. K.G. Ashar, Dr. D.R. Kerr, Dr. L.V. Gregor and Mr. A. Kran.

7.0 KEY TECHNICAL PERSONNEL

Dr. G.A. Silvey	man-hours	262.0 (project Supervisor)
Dr. V.Y. Doo		630.0
Mr. J.C. Hollis		248.5
Dr. D.R. Nichols		1467.8
Dr. D.R. Kerr		280.0

8.0 RECOMMENDATION FOR FUTURE WORK

8.1 SILICON NITRIDE MATERIALS RESEARCH - VAPOR GROWTH

IBM feels that a continuation of the current research and development on silicon nitride vapor growth techniques is important and should be continued. Specifically, the following work should be carried out:

8.1.1 The etch rates of silicon nitride in the literature are essentially for the nitride films that were deposited on homogeneously doped silicon substrates. In reality, for integrated circuit applications, the nitride films are often deposited on silicon substrates which have been entirely or partly precoated with oxide or glass. The etch rate of such nitride films may differ significantly from the ones in the literature. It is therefore, highly desirable to determine the etch rates of nitride films that were deposited on various substrates, e.g., N^+ or P^+Si, SiO_2, B_2O_3-SiO_2, and P_2O_5-SiO_2. Also the effect of post deposit anneal on the nitride etch rate should be investigated.

8.1.2 One of the most important characteristics of the silicon nitride is its extremely high resistance against impurity diffusion. Although its masking effect on the high temperature diffusion of common dopants has been reported, its ability

to resist the high temperature diffusion of common contaminants such as Na, K, Li, Cu and Au has yet to be investigated and the critical temperature, at which substantial diffusion may occur in nitride, should be determined.

8.1.3 Common contaminants such as Na and Cu are undesirable but are often present in many semiconductor devices. By applying silicon nitride at different processing steps, the source of the contaminants could be determined.

8.1.4 There are indications that some physical properties such as etch rate and dielectric constant of silicon nitride can be modified without seriously degrading its diffusion masking and passivation properties by suitable modification in the film composition. Detailed investigation should be made on film properties as a function of the film composition.

8.1.5 To optimize silicon nitride for sophisticated device structures, significant material research is required to arrive at:

a. Proper deposition rate
b. Temperature
c. Etching rate

Since all these three properties are related to material and electrical characteristics, a continuous interchange of information between materials work and circuit application is absolutely necessary and hence proposed.

8.2 APPLICATION TO EXPERIMENTAL DEVICE STRUCTURES

Simultaneously, with the further development of the material, effort now, also, should be directed towards applying the silicon nitride to experimental integrated circuit structures. Hence, relatively high speed integrated circuits, utilizing NPN double diffused transistors and IGFET circuits should be used as test vehicles.

8.3 RELIABILITY EVALUATION

A set of test procedures for evaluating the passivation capability for each type of IC circuits should be worked out.

Measurements should be made based upon the test procedure mentioned above and the results of this reliability testing will be interpreted in terms of available mathematical models on surface charge phenomenon and impurity instability.

Presently it also appears that a number of other reliability tests in terms of successive nitride depositions should be made to better evaluate the application of Si_3N_4. For instance, some of the experimental variations should be to deposit Si_3N_4 at various stages during the processing of devices. Also, the effect of phosphosilicate glass and borosilicate glass formed during diffusions on Si_3N_4 should be analyzed.